

COMPAL CONFIDENTIAL

MODEL NAME : VAR10

PCB NO : LA-9781P

BOM P/N : 4319ME31L01

GPIO MAP: GPIO map rev 3.0C

P5 17

REV : 0.2 (X01)

2013.01.17

@ : Nopop Component

CONN@ : Connector Component

PXDP@,JTAG@ : Total debug Component (pop them until ST)

MB PCB	
Part Number	Description
DAA0006H000	PCB 0W2 LA-9781P REV0 M/B

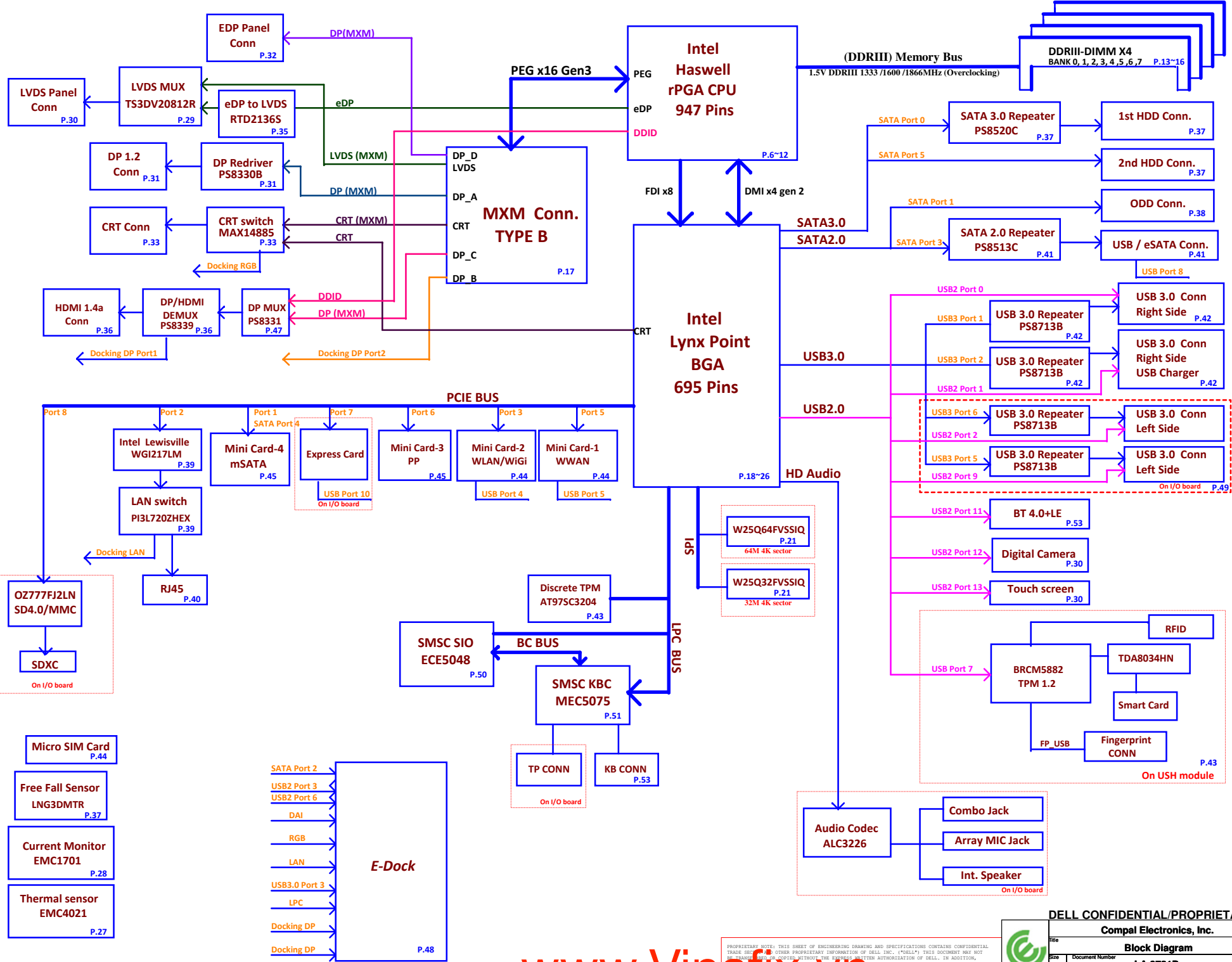
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN +3.3V_MXM +5V_MXM	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD 1
SATA 1	ODD
SATA 2	Dock
SATA 3	ESATA
SATA 4	mSATA
SATA 5	HDD 2

USB PORT#	DESTINATION
0	JUSB1 (Ext Right Side)
1	JUSB2 (Ext Right Side)
2	IO Board- JUSB1 (Ext Left Side)
3	Docking USB3.0
4	WLAN/WIMAX
5	WWAN/UWB
6	Docking USB 2.0
7	USH
8	ESATA
9	IO Board- JUSB2 (Ext Left Side)
10	Express Card
11	BT 4.0
12	Carmera
13	Touch Screen

USH		
	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-4 (NVRAM)
Lane 2	10/100/1G LOM
Lane 3	MINI CARD-2 (WLAN)
Lane 4	NA
Lane 5	MINI CARD-1 (WWAN)
Lane 6	MINI CARD-3 (PP)
Lane 7	EXPRESS CARD
Lane 8	MMI(Card reader)

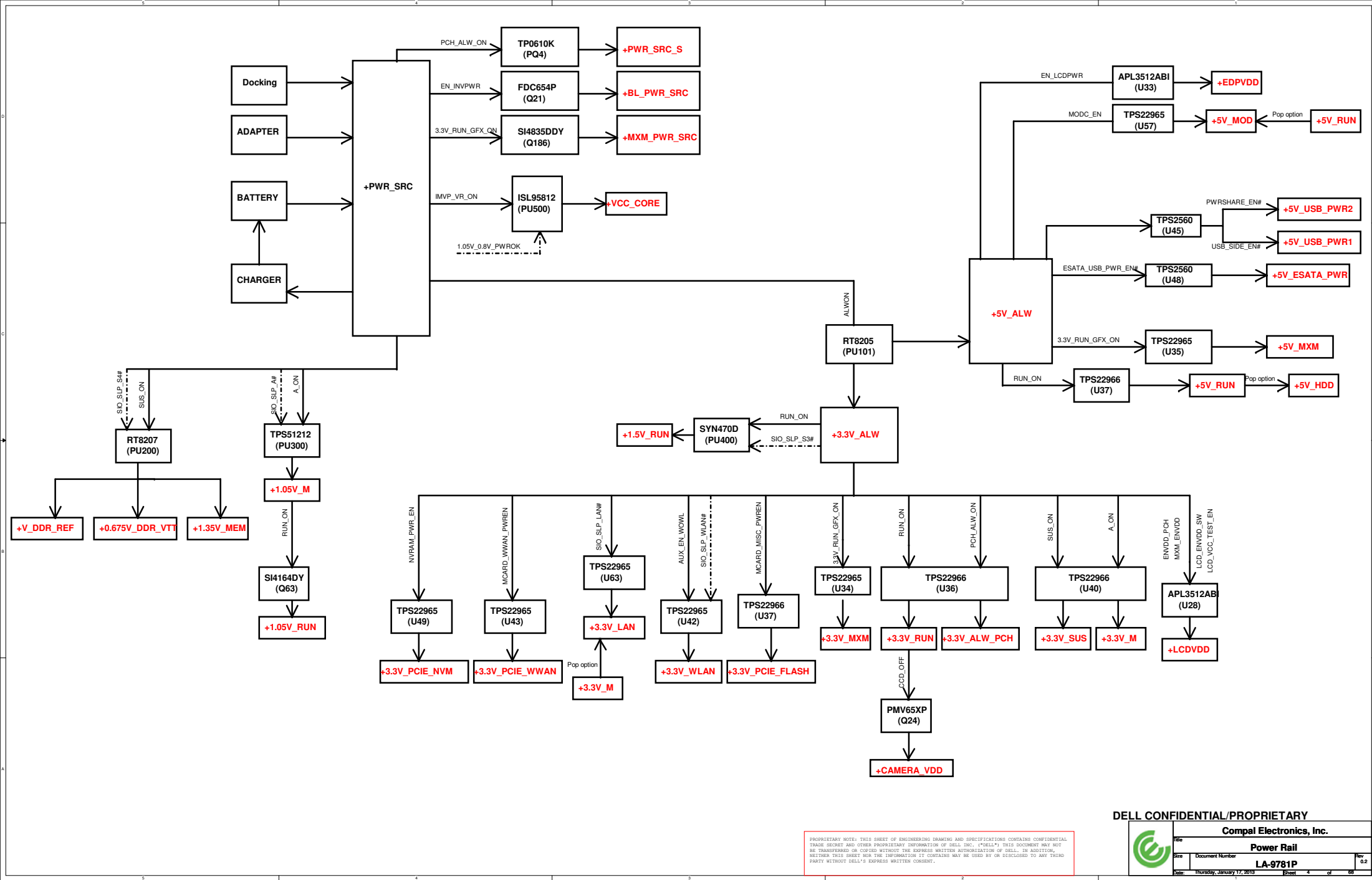
Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top		Copper foil	0.5oz
		3.7	Prepreg	1080
2	GND1		Copper foil	1oz
		3.7	Core	4mil
3	Sig 1		Copper foil	1oz
		3.9	Prepreg	1080H+2116H
4	GND/PWR		Copper foil	2oz
		3.7	Core	4mil
5	Sig 2		Copper foil	1oz
		3.8	Prepreg	1080Hb2
6	Sig 3		Copper foil	1oz
		3.7	Core	4mil
7	GND/PWR		Copper foil	2oz
		3.9	Prepreg	1080H+2116H
8	Sig 4		Copper foil	1oz
		3.7	Core	4mil
9	GND 3		Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	
Overall Thickness (1.45mm ± 10%)				57.09

USB3.0	DESTINATION
Port 1	JUSB1 (Ext Right Side)
Port 2	JUSB2 (Ext Right Side)
Port 3	Dock
Port 4	NA
Port 5	IO Board- JUSB2
Port 6	IO Board- JUSB1

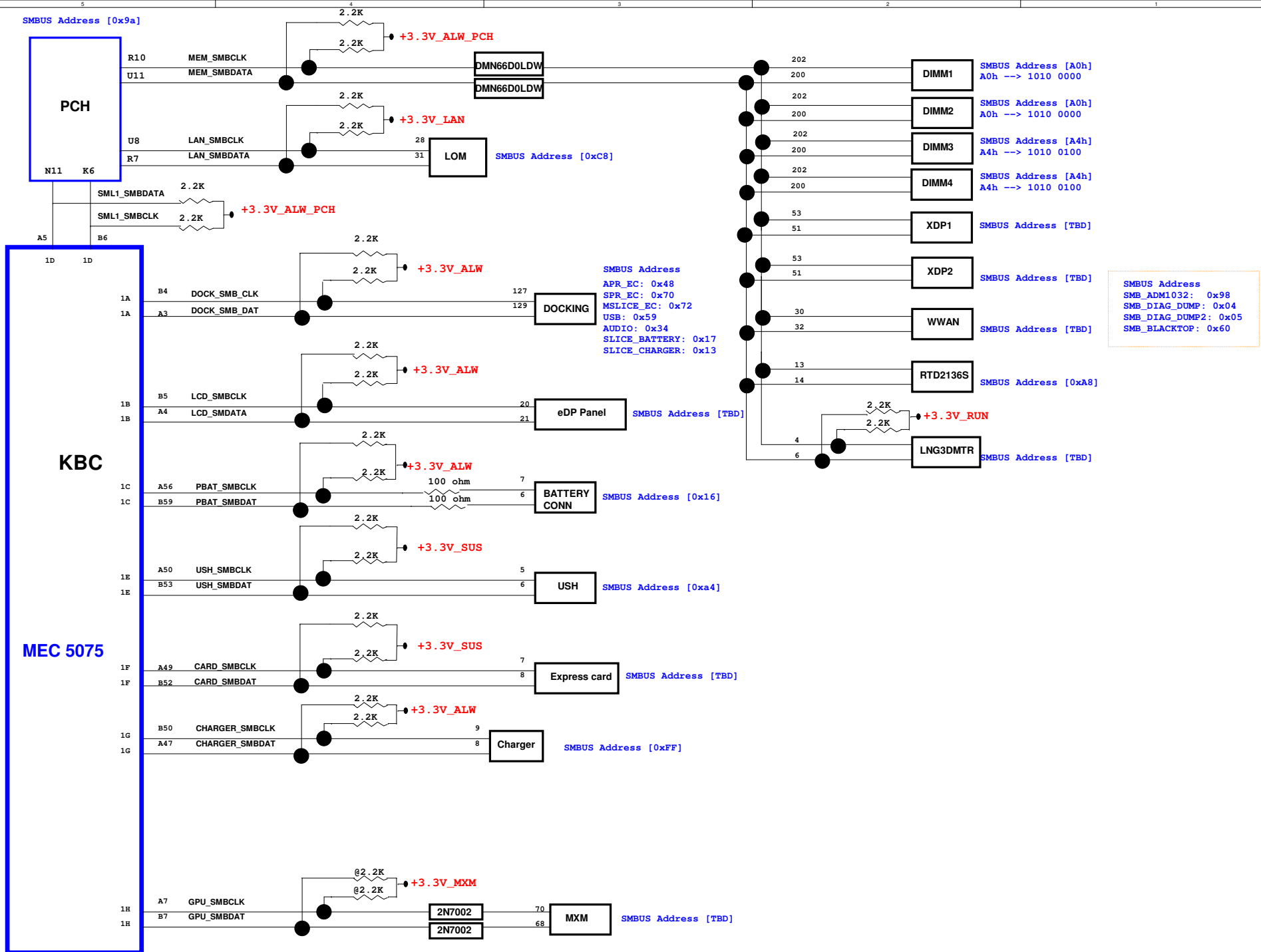
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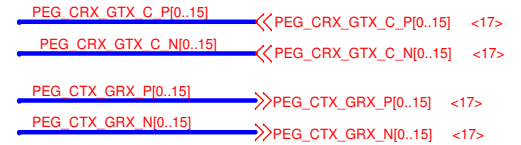
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Index and Config.			
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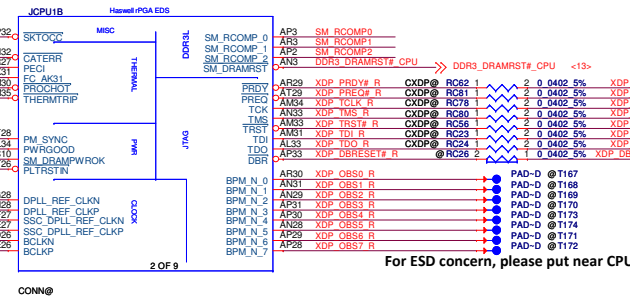
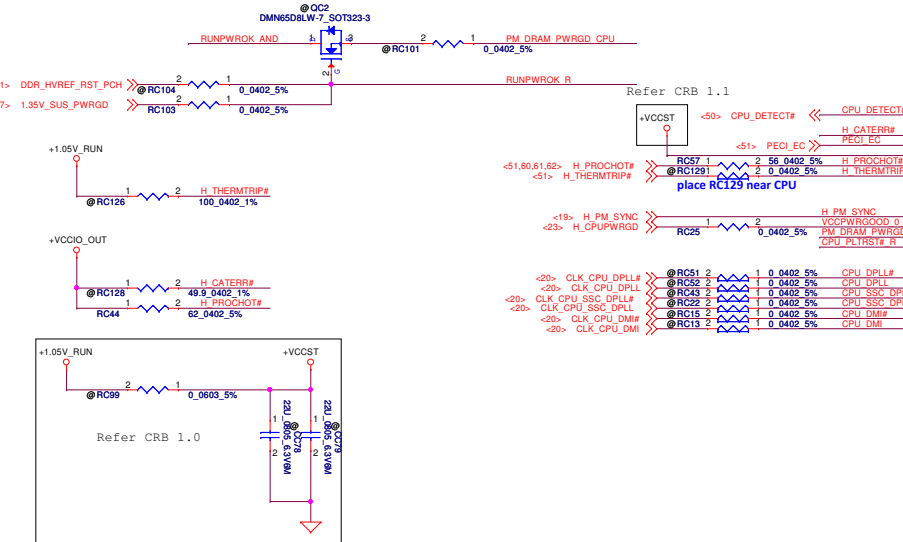
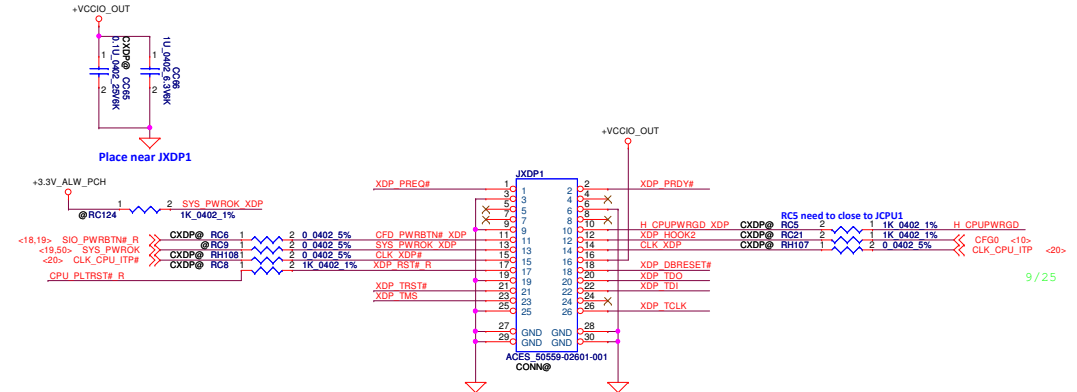
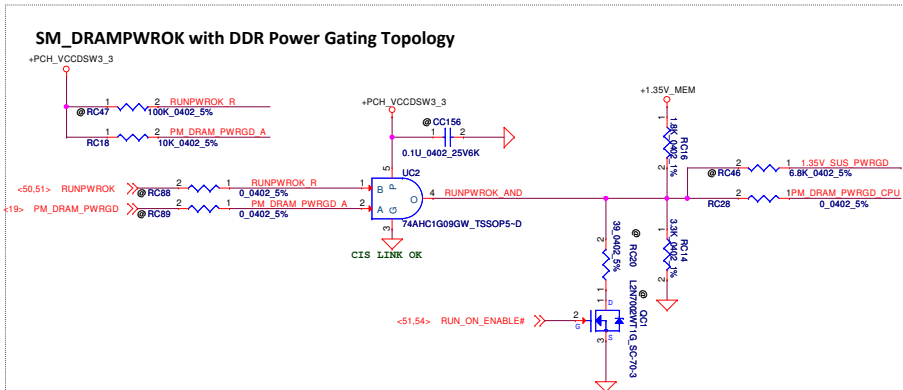




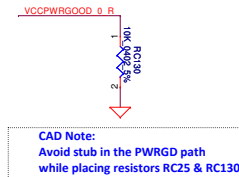
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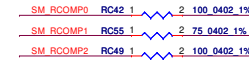


For ESD concern, please put near CPU



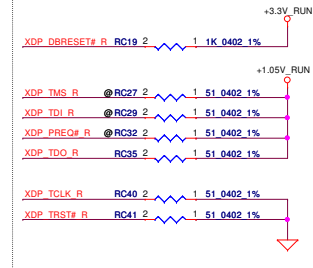
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

DDR3 COMPENSATION SIGNALS

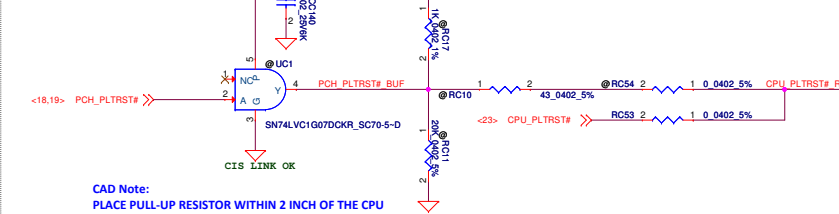


CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

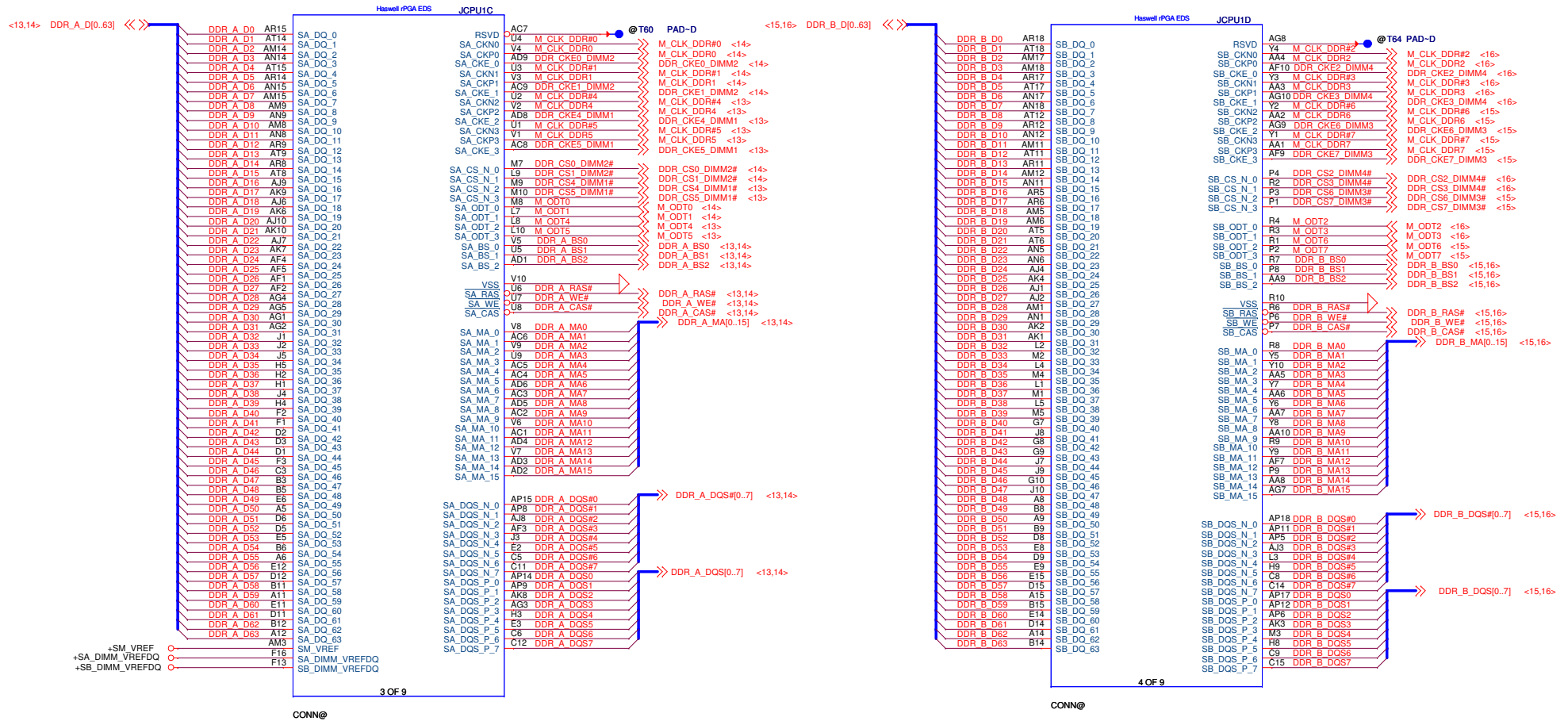
PU/PD for JTAG signals



Buffered reset to CPU



CAD Note:
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU



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Haswell (3/7)

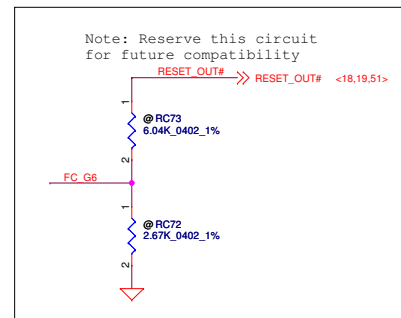
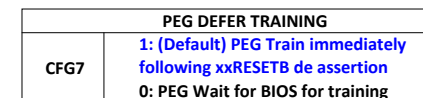
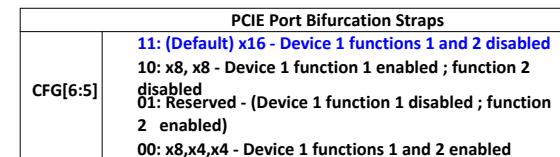
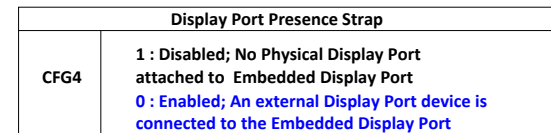
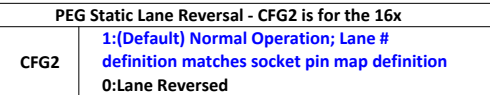
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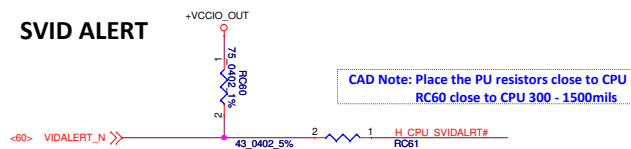
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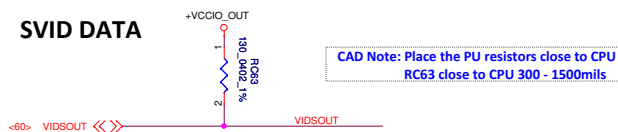
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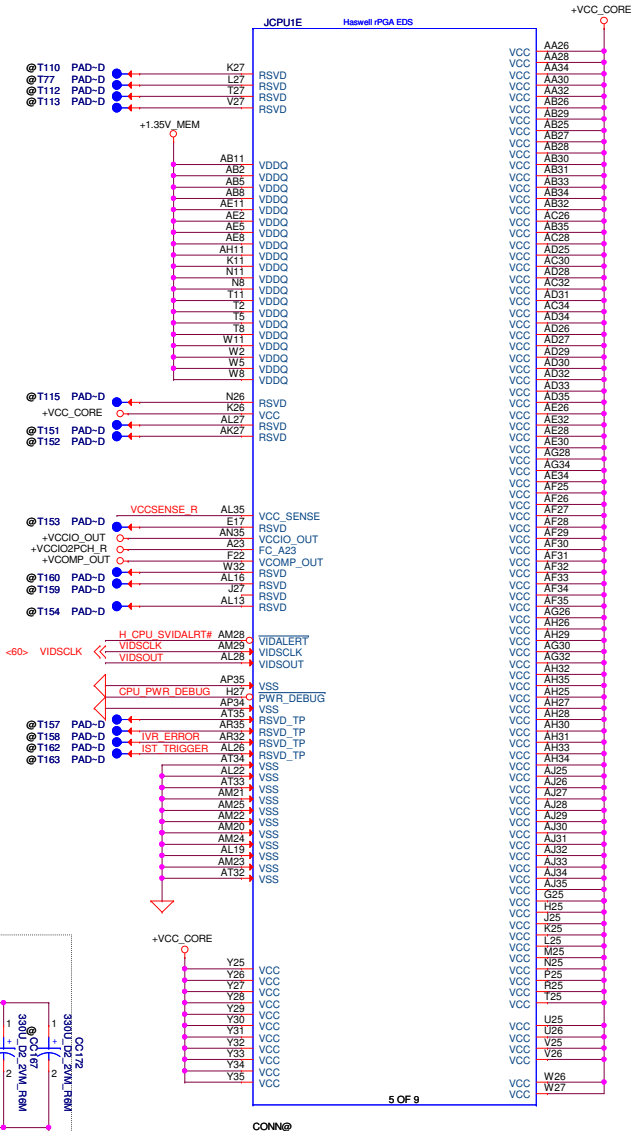
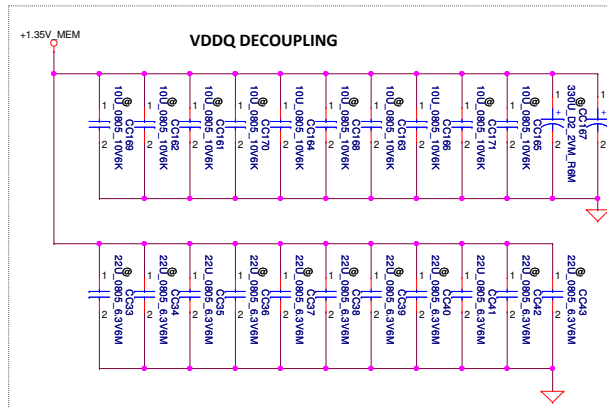
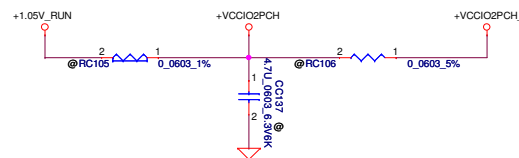
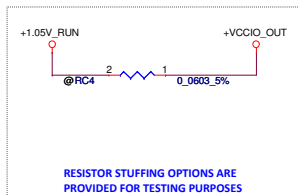
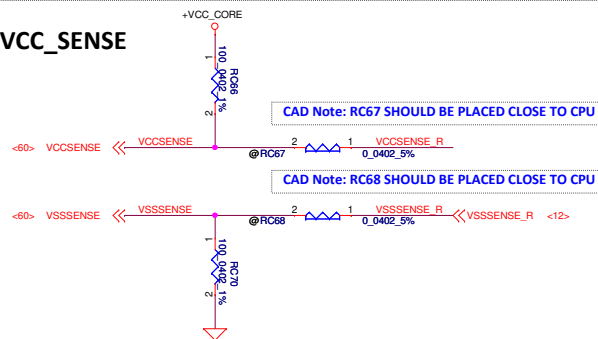
SVID ALERT

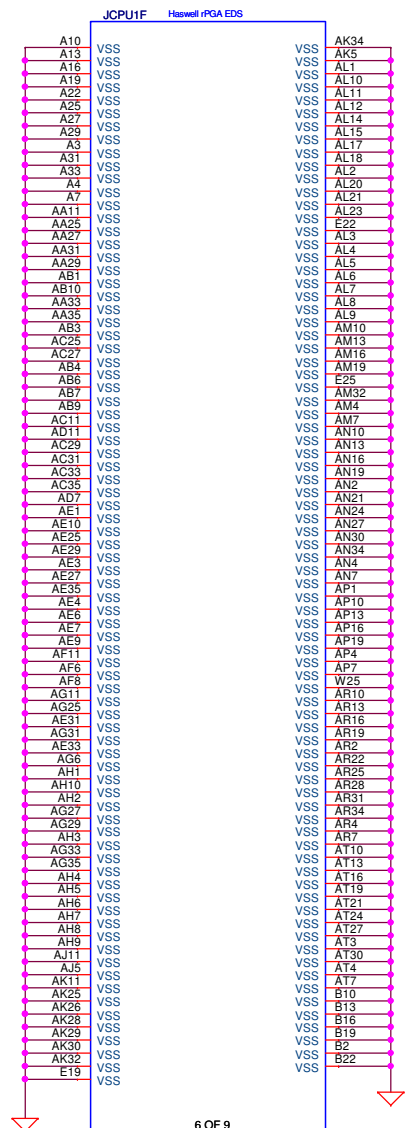


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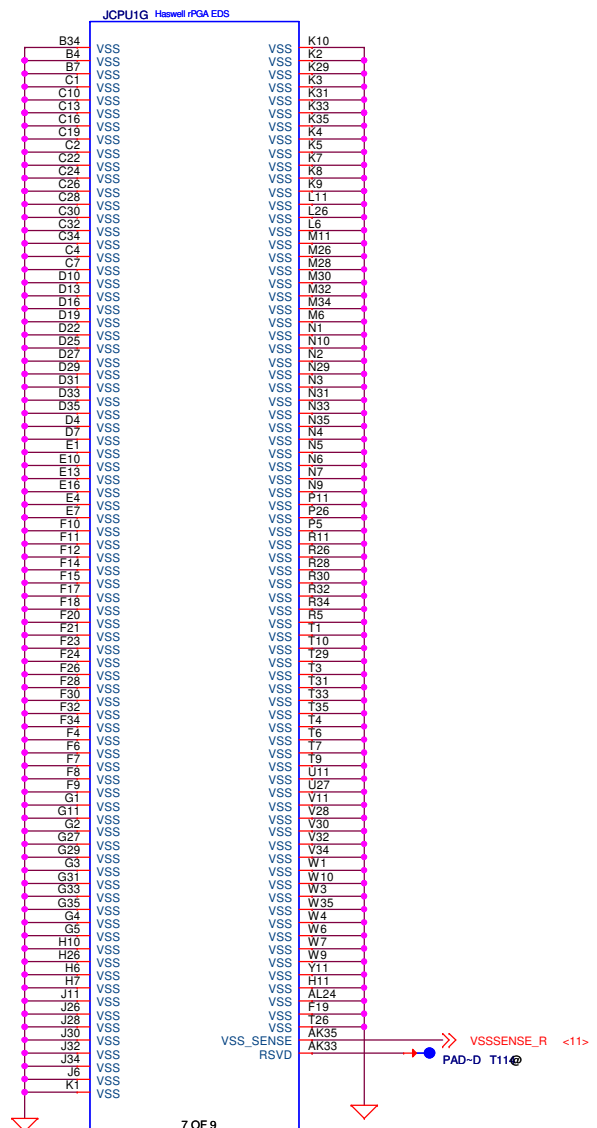


VCC_SENSE





CONN@



CONN@

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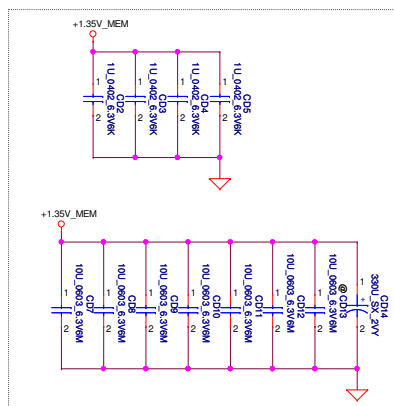
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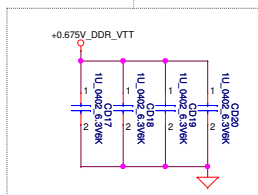
Populate RD1, De-Populate RD2 for Intel DDR3
VREFDQ multiple methods M1

Populate RD2, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

```
<14,8> DDR_A_DQS#[0..7] <<>>
<14,8> DDR_A_DQS[0..7] <<>>
<14,8> DDR_A_D[0..63] <<>>
<14,8> DDR_A_MA[0..15] <>>
```



Layout Note:
Place near JDIMM1.203,204

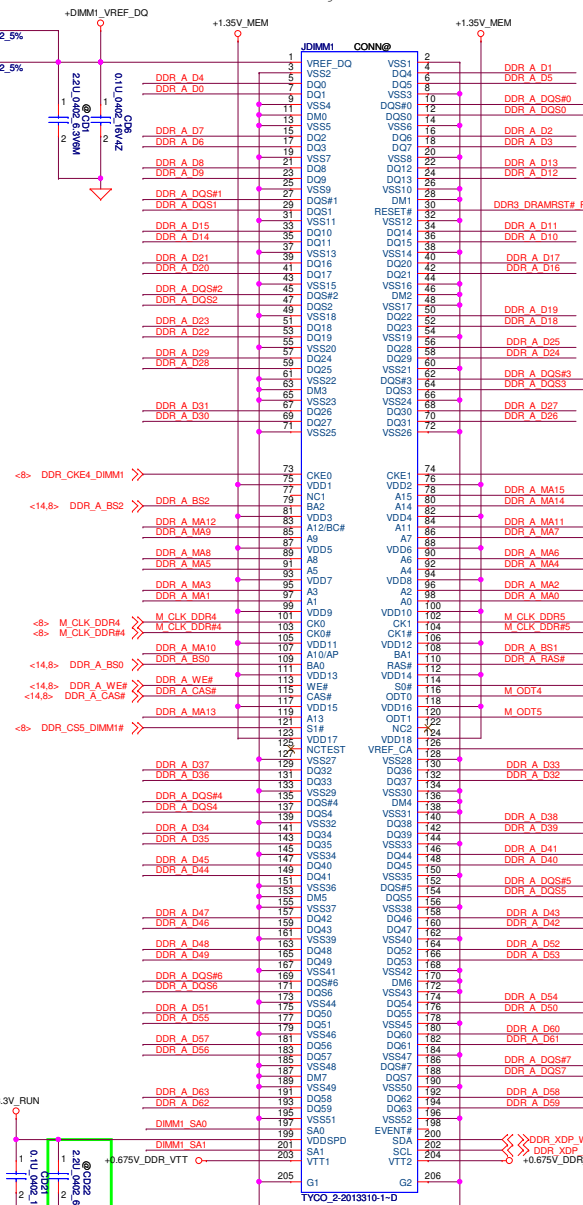


DIMM Select

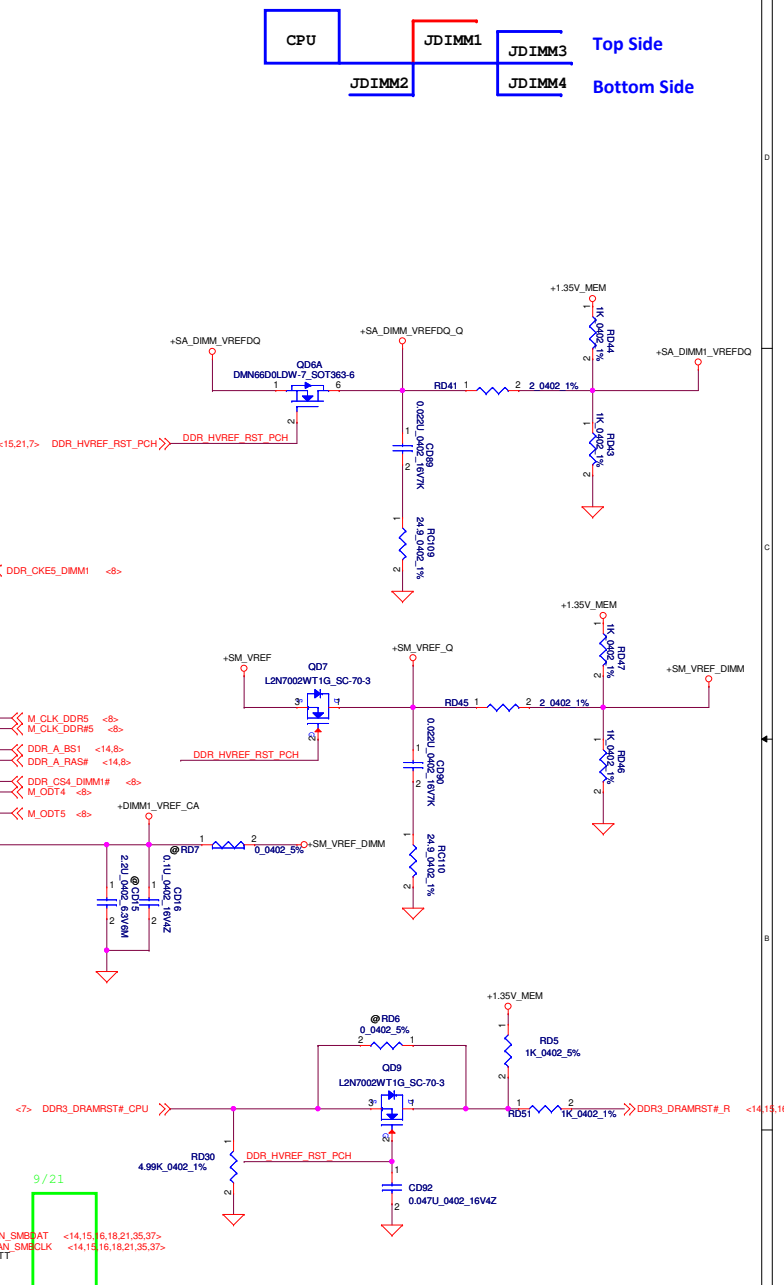
	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1

JDIMM1 STD Type H=9.2

PN change to SP07000NB10



Check D15 de-pop



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DDR3L-SODIMM SLOT1

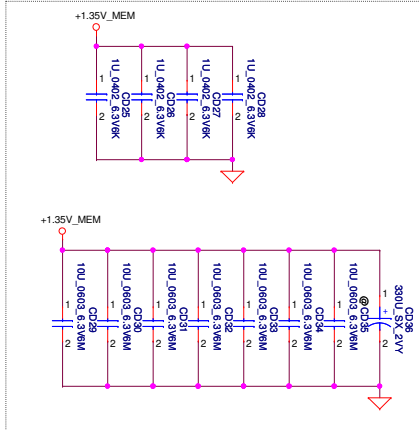
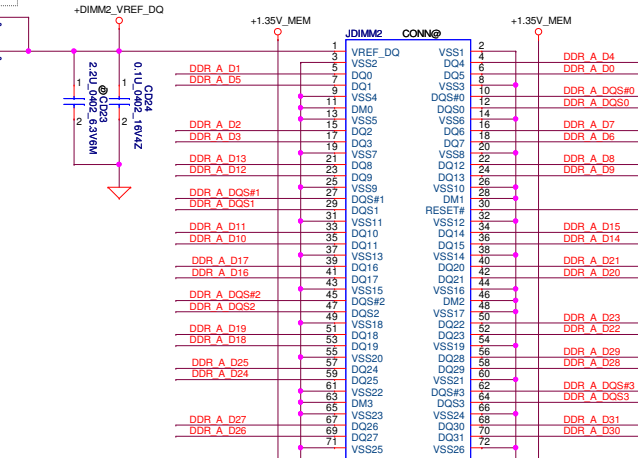
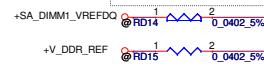
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JDIMM2 STD Type H=5.2

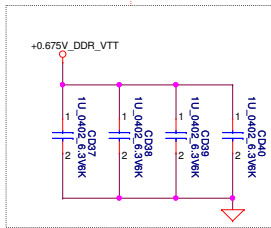
PN change to SP070000F00

All VREF traces should have 10 mil trace width

<13.8> DDR_A_DQS#[0..7] <<>
<13.8> DDR_A_DQS#[0..7] <<>
<13.8> DDR_A_DQ[0..63] <<>
<13.8> DDR_A_MA[0..15] <<>

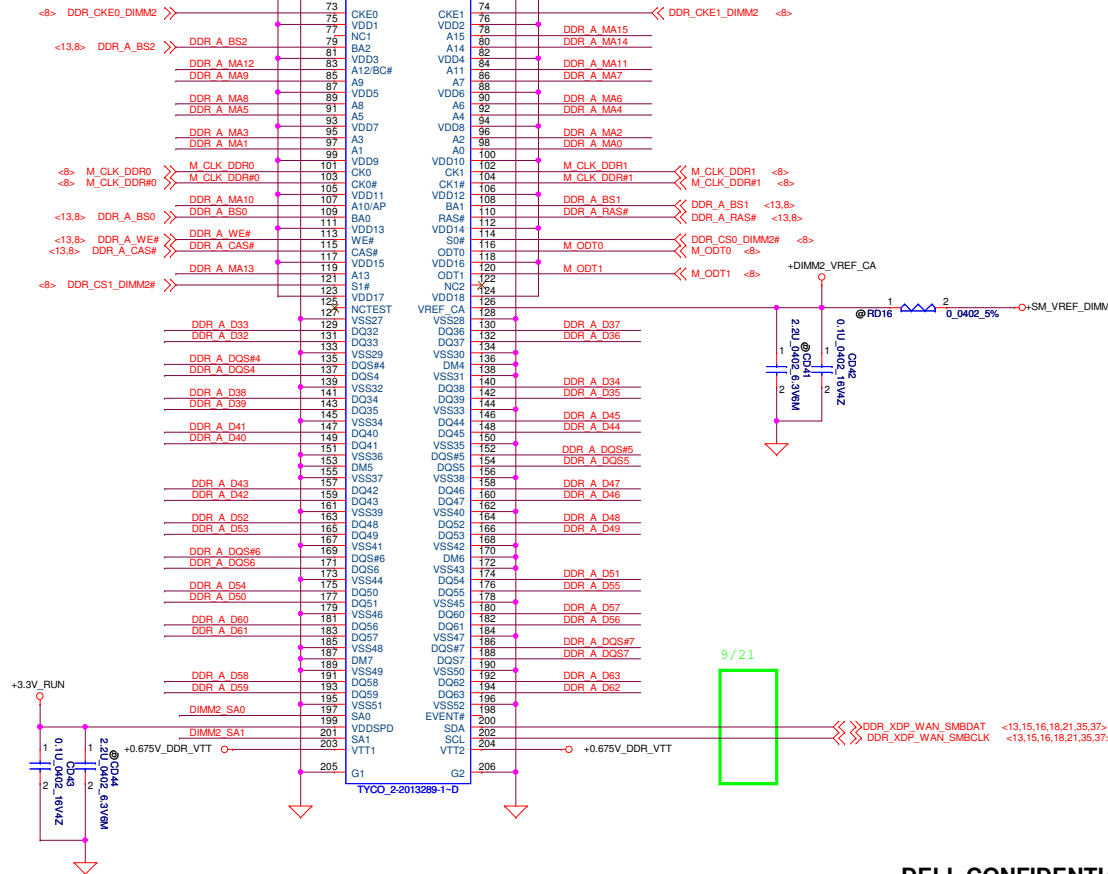
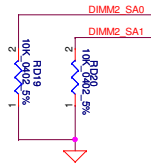


Layout Note:
Place near JDIMM2.Pin 203,204



DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1



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DDRIII-SODIMM SLOT2

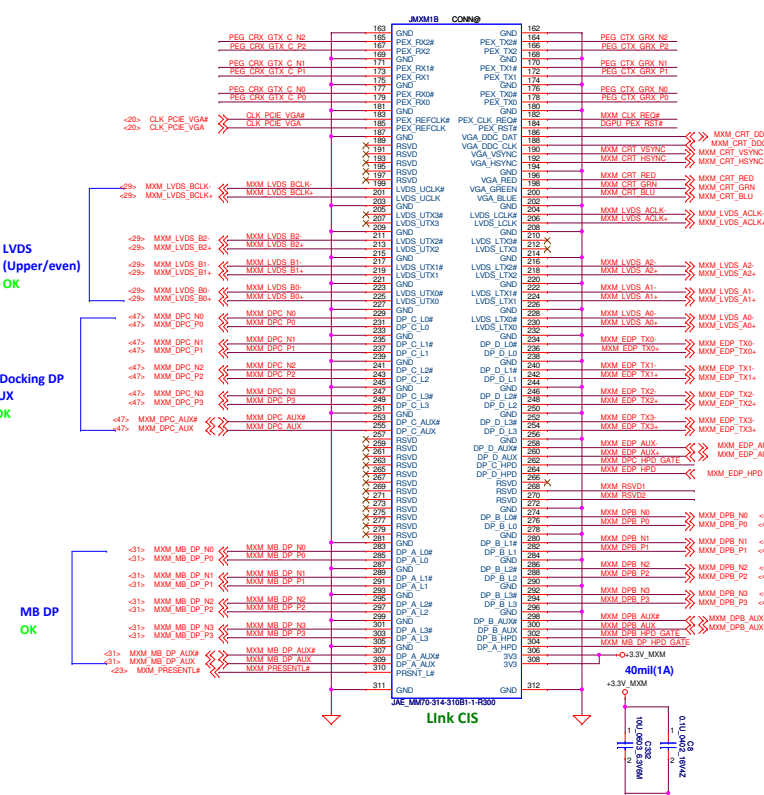
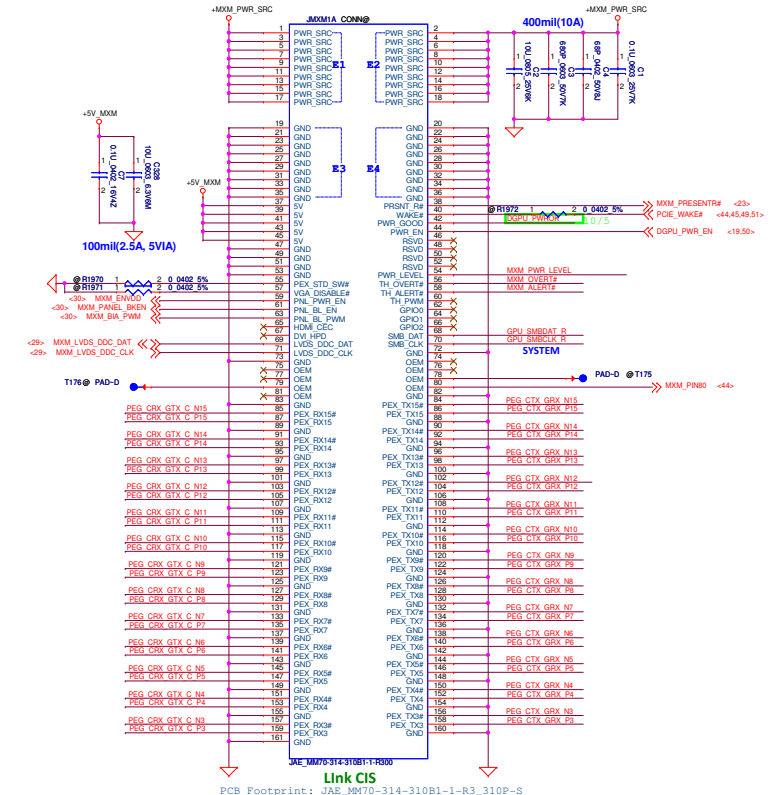
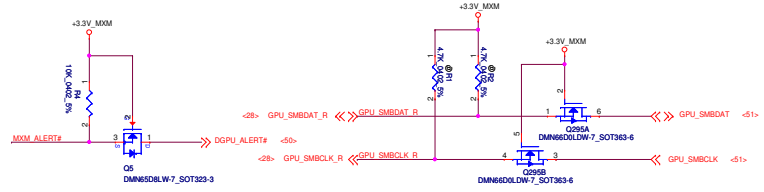
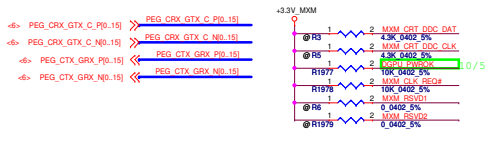
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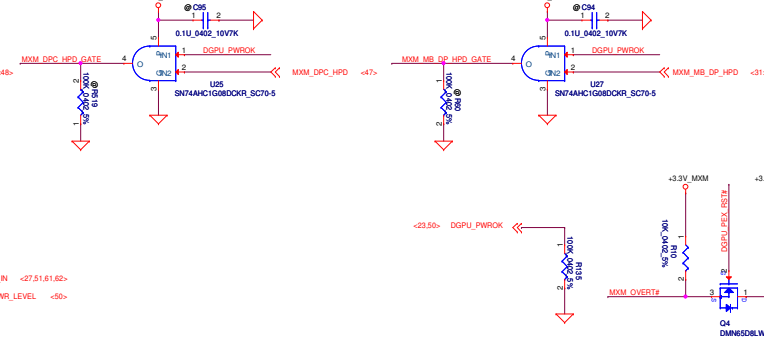
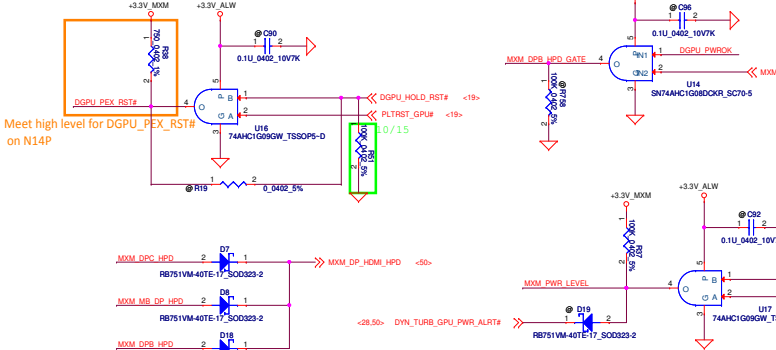


CRT
OK

LVDS
(Lower/odd)
OK

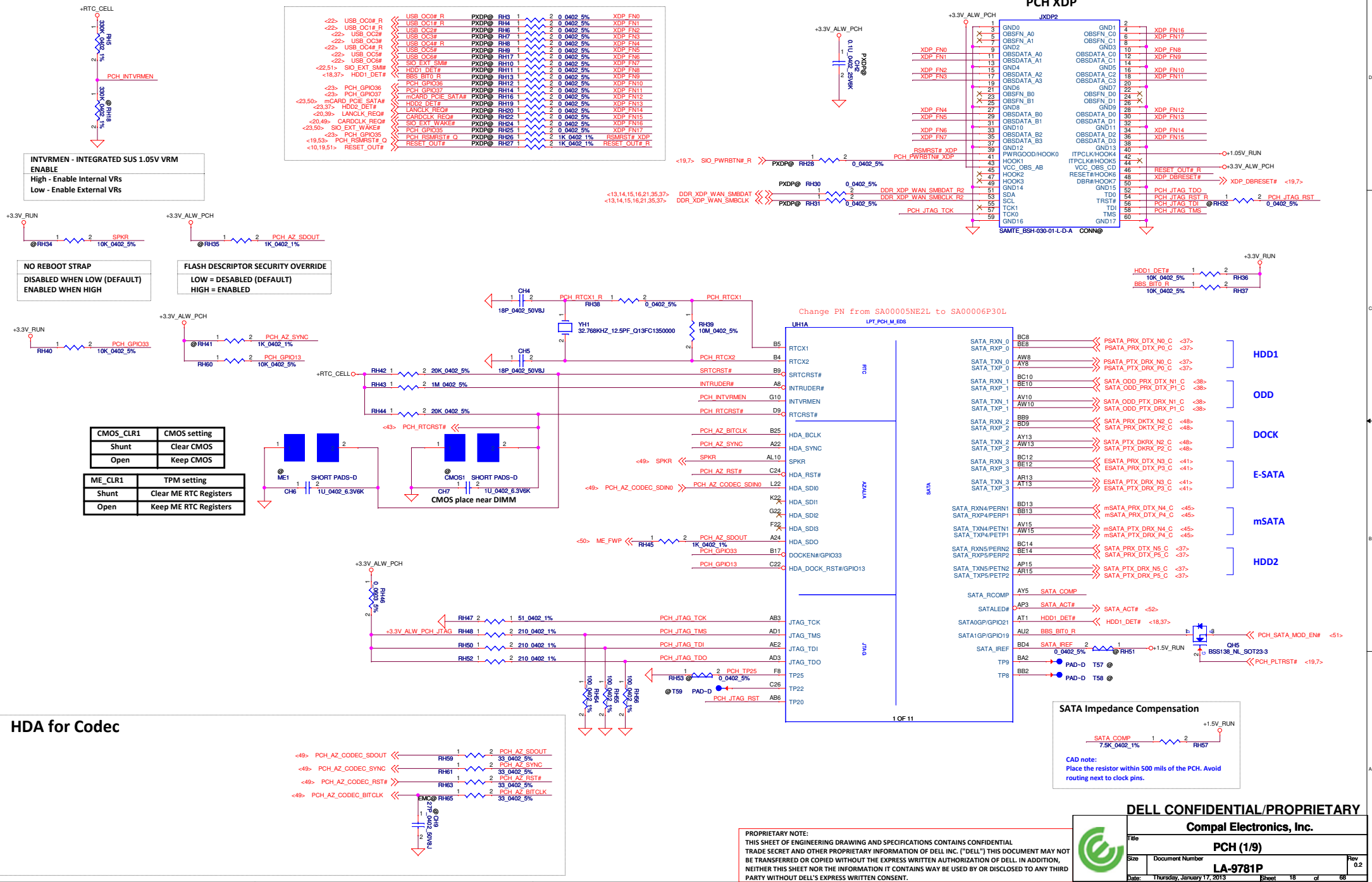
eDP
OK

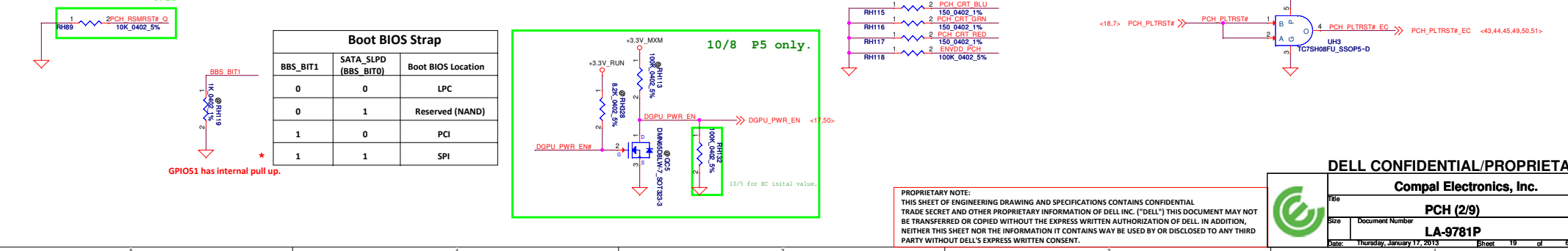
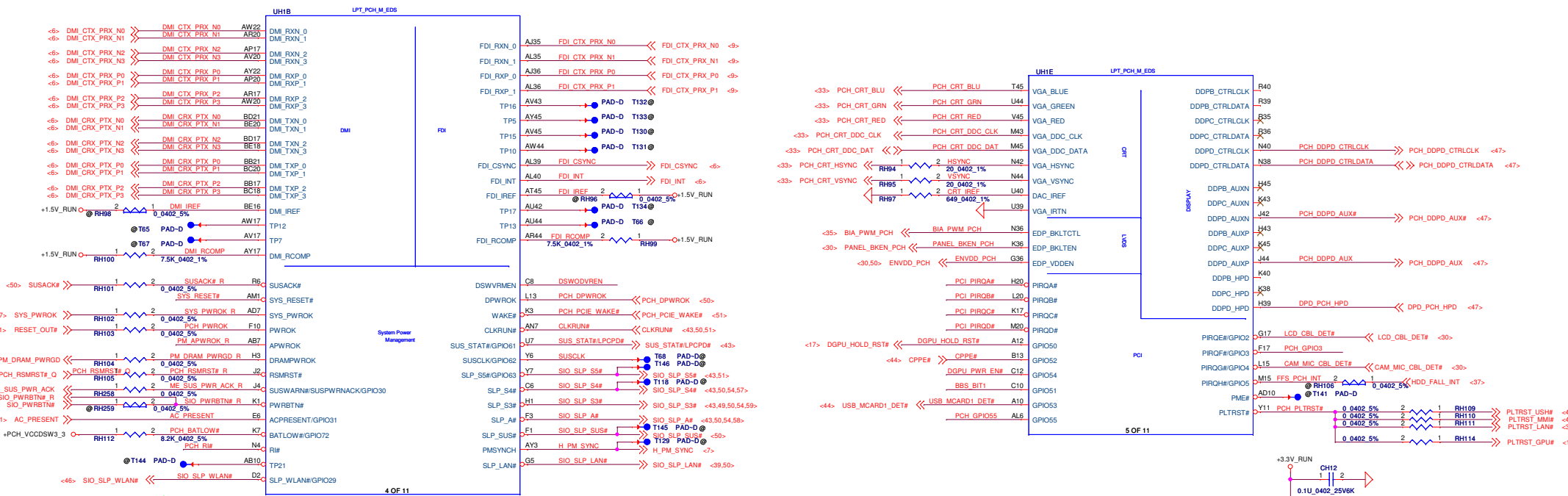
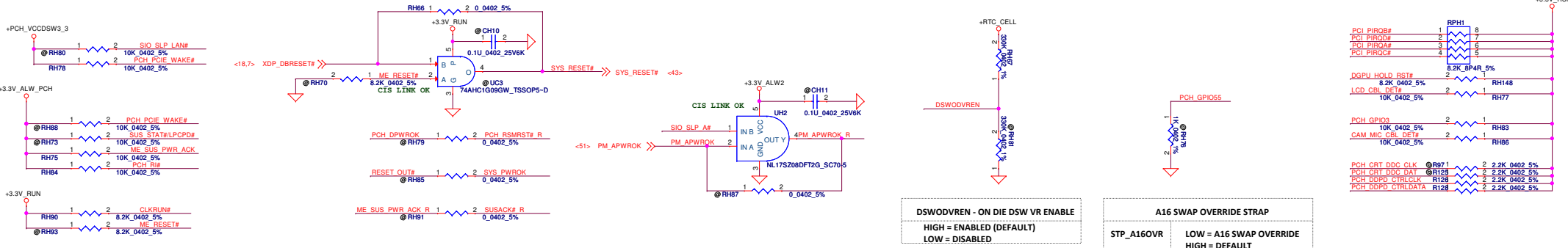
Docking DP port 2
OK

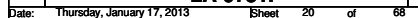
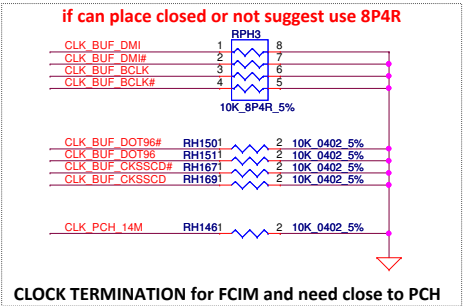


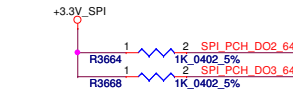
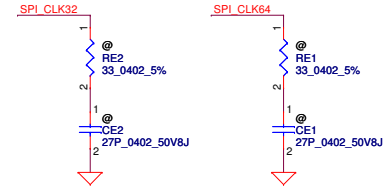
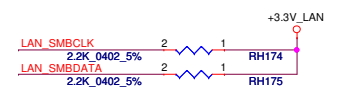
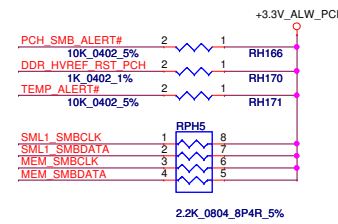
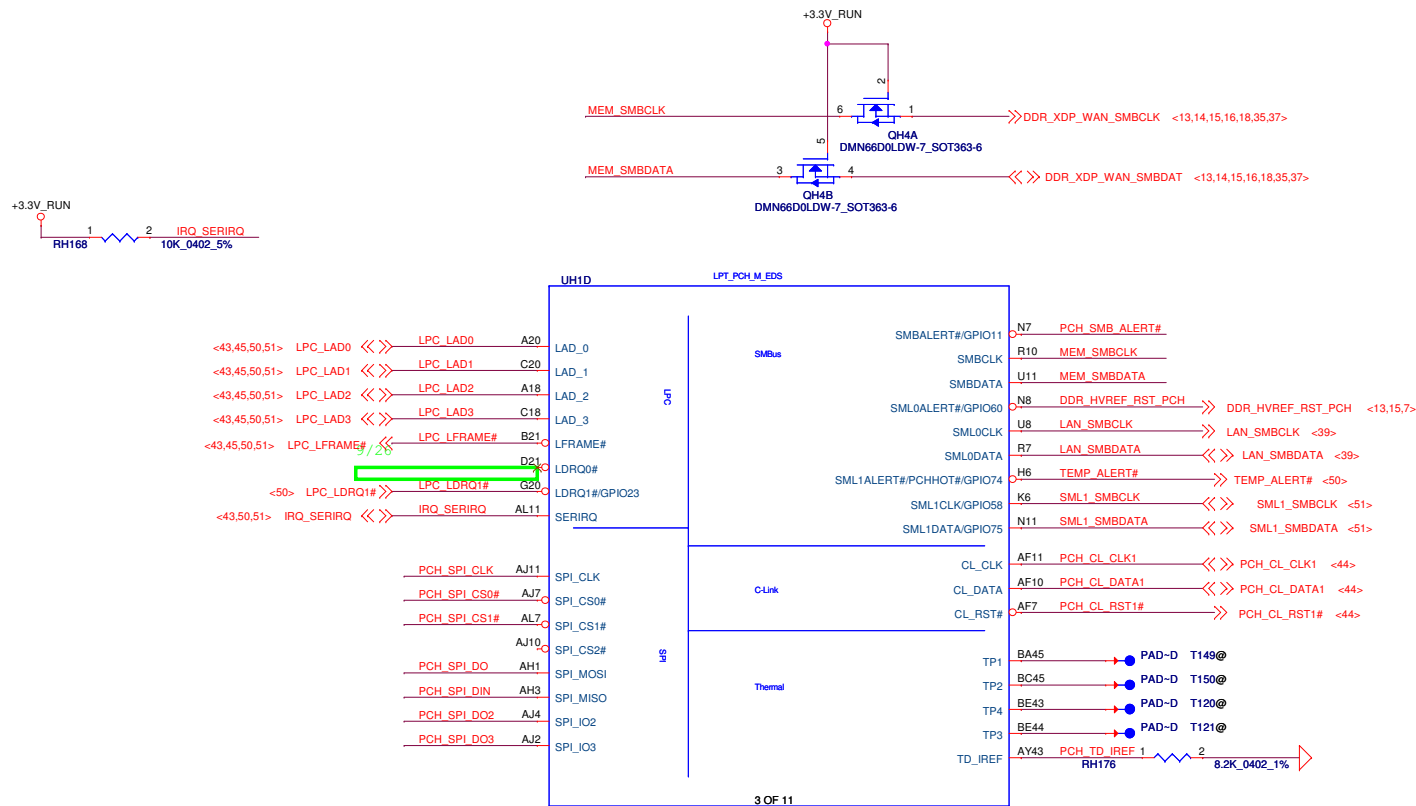
Link CIS

PCB Footprint: JAE_MM70-314-310B1-1-R3_310P-S

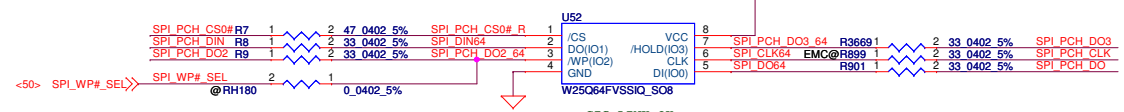




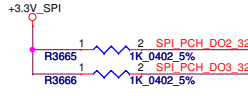




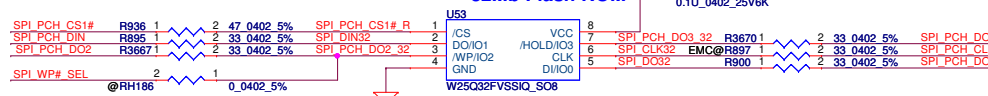
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64Mb Flash ROM



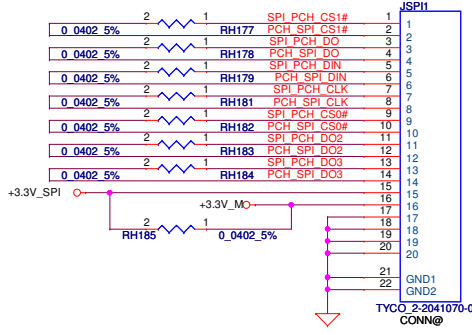
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200 MIL SO8
32Mb Flash ROM



U53 change PN to SA00003K820 IC FL 32M W25Q32FVSSIQ SOIC 8P SPI ROM



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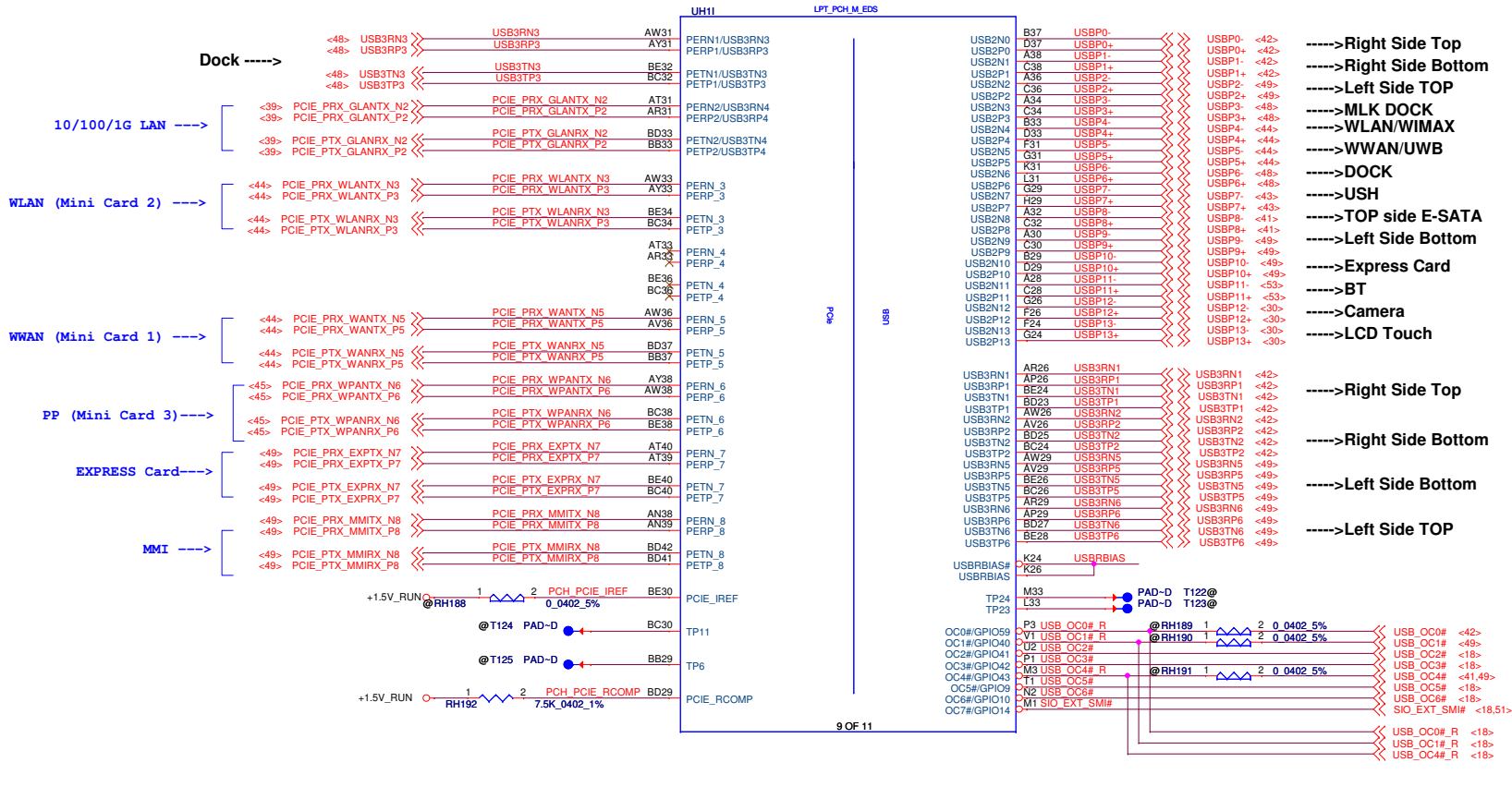
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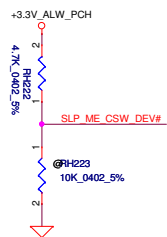
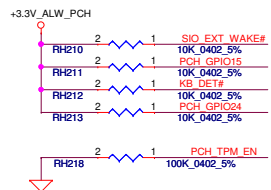
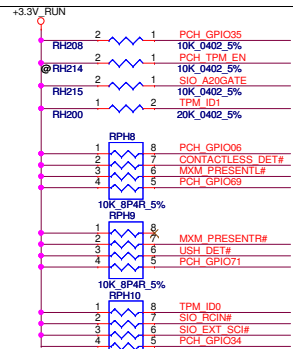
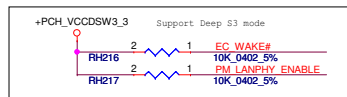


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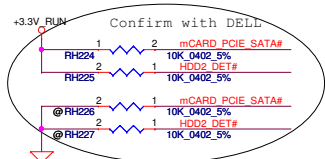
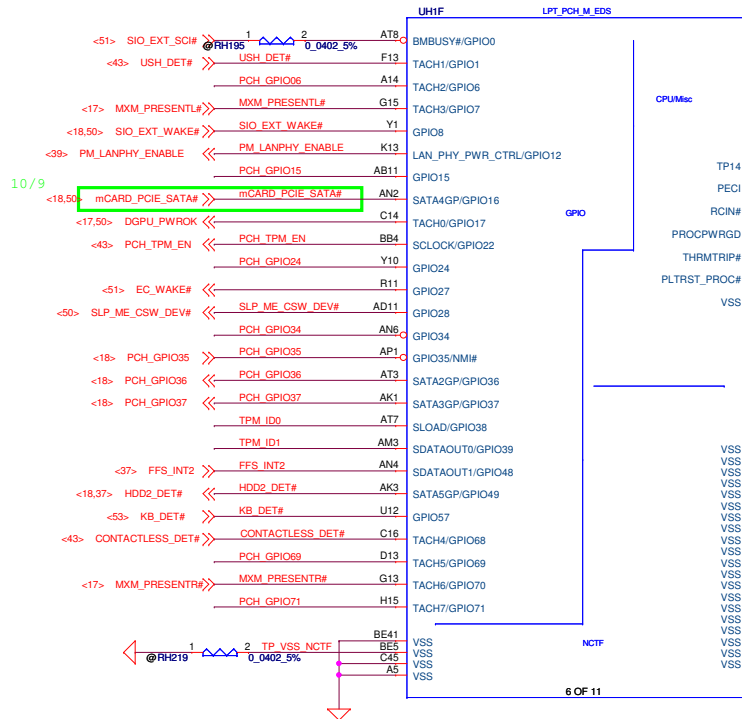
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PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW

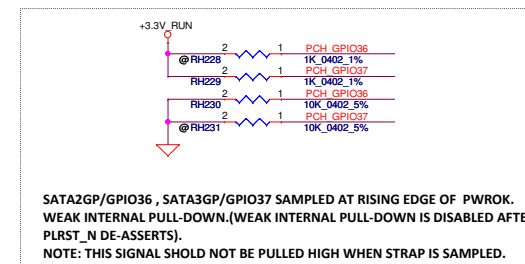


Note: GPIO strap option is only available for SATA/PCIE muxed signals to support mSATA/mini PCIE port switching

GPIO16	GPIO49
0: PCIE1	0: PCIE2
1: SATA4	1: SATA5

00b or 01b: Assign muxed signal to desired port
10b: Reserved
11b: Assign desired port based on GPIO

Fixed Signals				Muxed Signals				Fixed Signals				Muxed Signals				Fixed Signals			
USB3_1	USB3_2	USB3_5	USB3_6	PCIE1_1	PCIE1_2	PCIE1_3	PCIE1_4	PCIE1_5	PCIE1_6	PCIE1_7	PCIE1_8	SATA4_1	SATA4_2	SATA4_5	SATA4_0	SATA5_1	SATA5_2	SATA5_3	SATA5_4
1	2	5	6	(00)	(00)	3	4	5	6	7	8	(00)	(00)	4	5	0	1	2	3
				USB3_3	USB3_4							PCIE1_1	PCIE1_2						
				(01)	(01)							(01)	(01)						



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PCH (6/9)

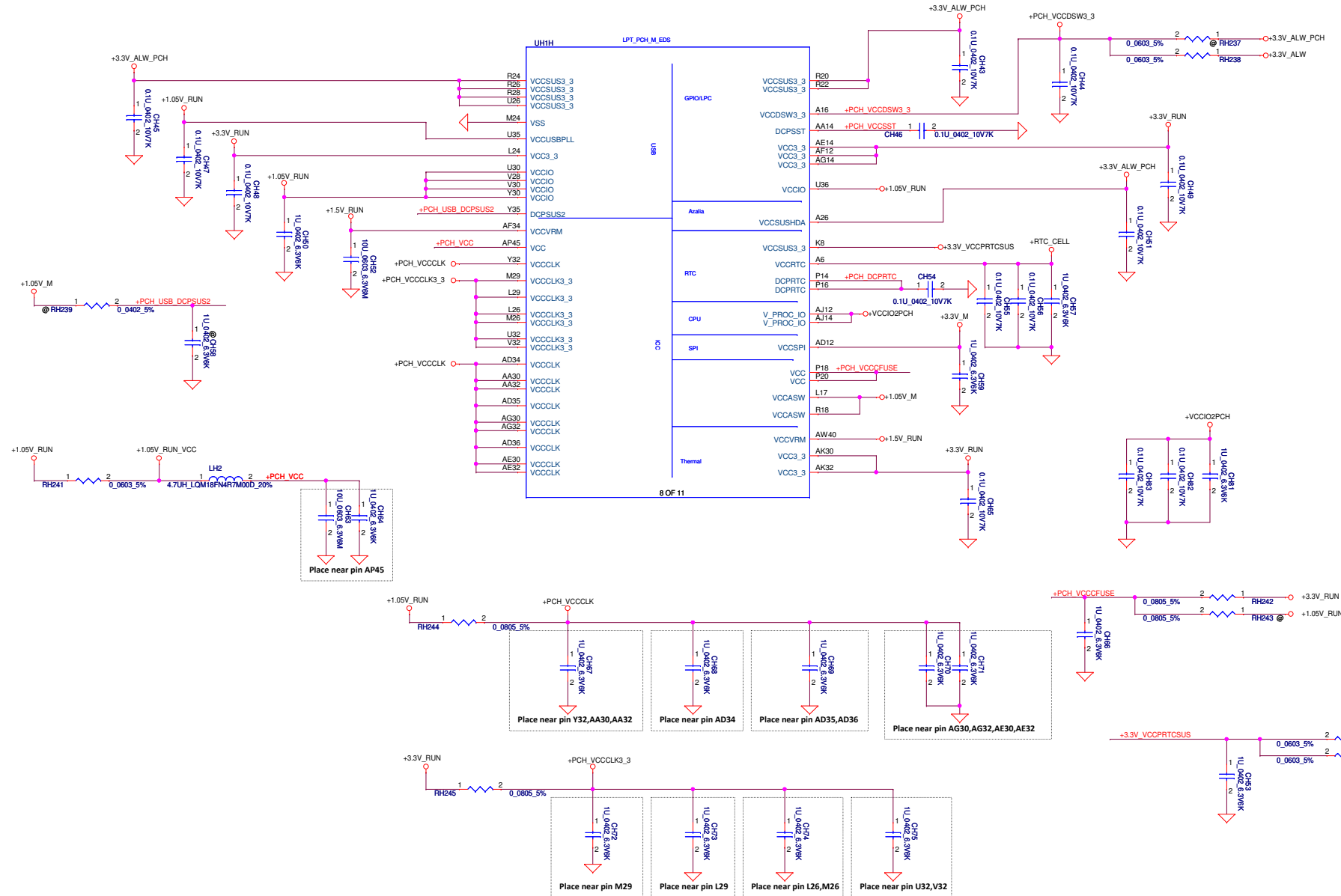
LA-9781P

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Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

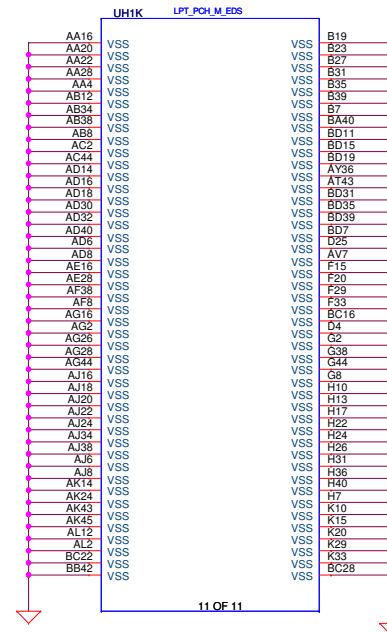
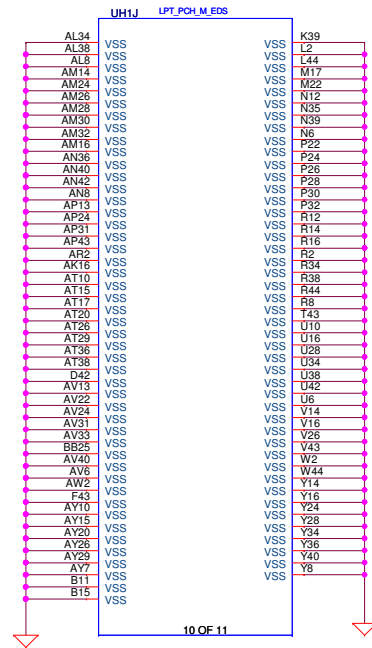
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Diagram illustrating the JFANI connector connections for the ACES_50271-0040N-001 module. The connections are as follows:

- FAN1_PWM (Signal) connects to JFANI CONN@ Pin 1.
- FAN1_TACH_FB (Signal) connects to JFANI CONN@ Pin 2.
- +5V_RUN (Power) connects to JFANI CONN@ Pin 3.
- GND1 (Ground) connects to JFANI CONN@ Pin 4.
- GND2 (Ground) connects to JFANI CONN@ Pin 5.

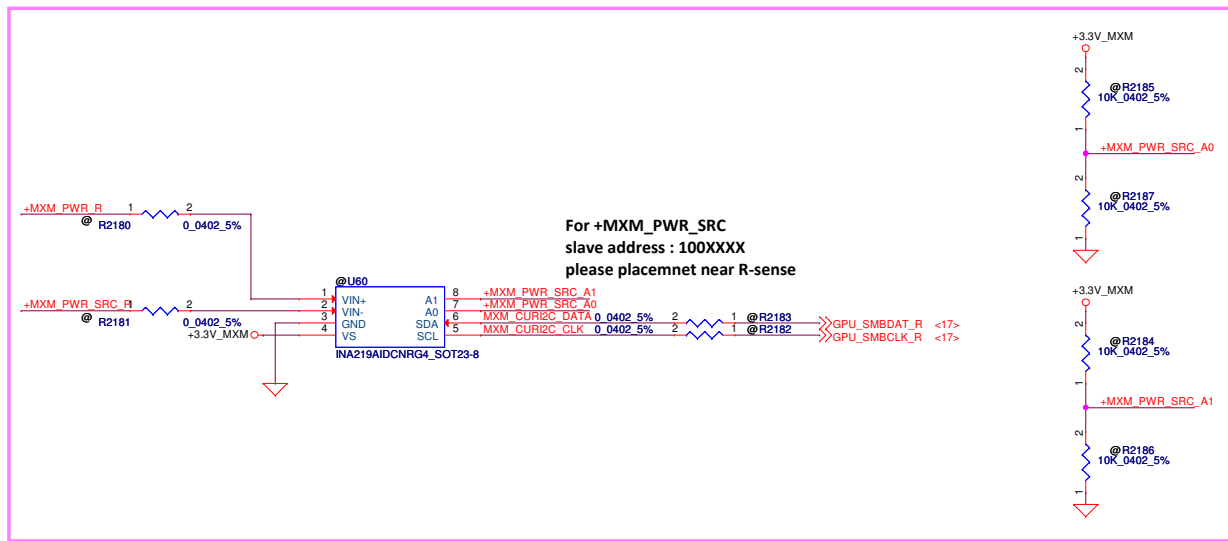
The module is labeled ACES_50271-0040N-001. The status "Link CIS OK" is indicated in green.

[illegible][illegible]

Rest=1.33k, Tp=93degree

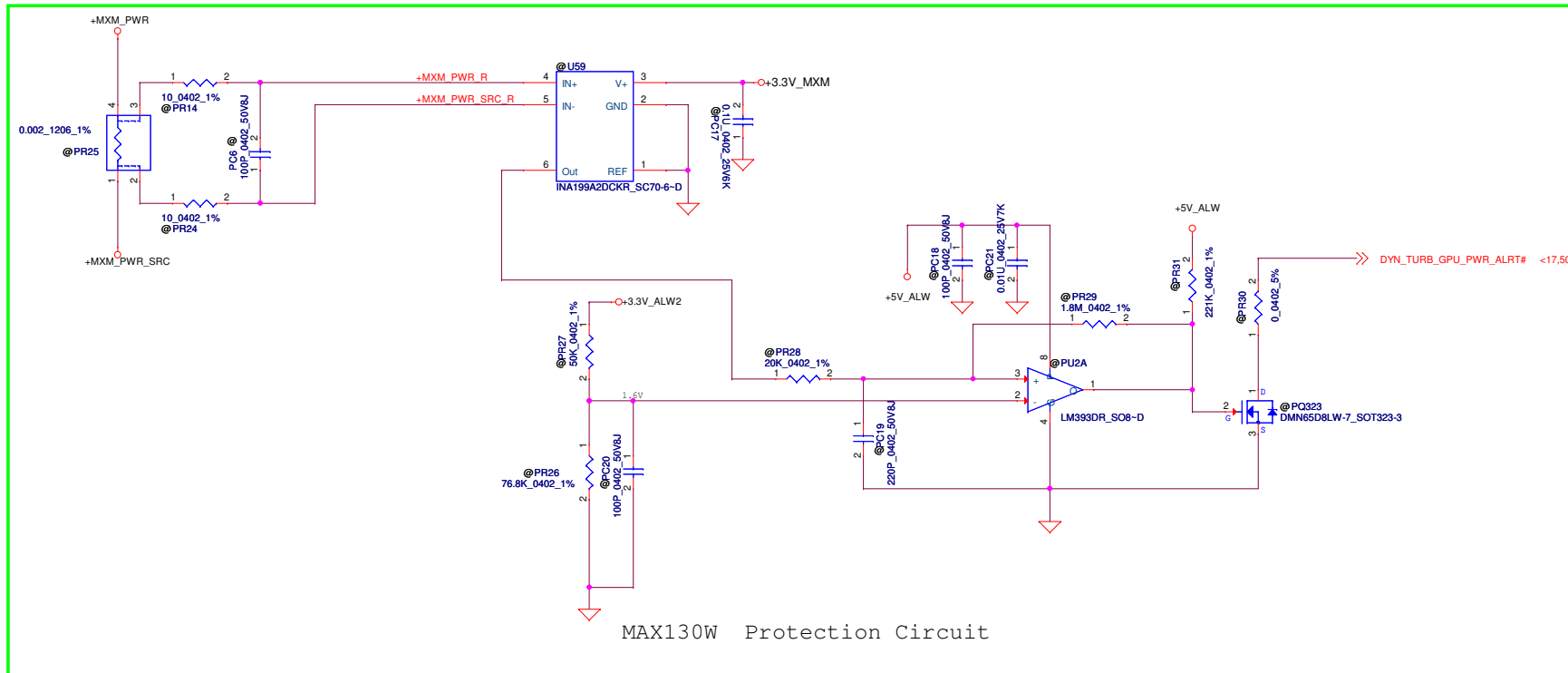
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Monitor PWR_SRC_MXM



RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)
100	1001_101(r/w)
180	1001_110(r/w)
300	1001_111(r/w)
430	1001_000(r/w)
560	1001_001(r/w)
750	1001_010(r/w)
1270	1001_011(r/w)
1600	0101_000(r/w)
2000	0101_001(r/w)
2700	0101_010(r/w)
3600	0101_011(r/w)
5600	0101_100(r/w)
9100	0101_100(r/w)
20000	0101_101(r/w)
Open	0011_000(r/w)

Monitor PWR_SRC_MXM for DELL request



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Current Sensor

LA-9781P

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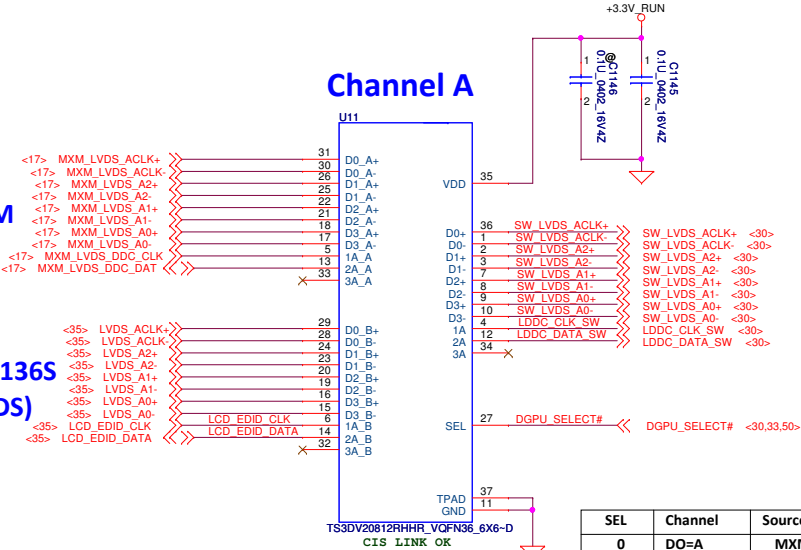
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From MXM

From RTD2136S
(eDP to LVDS)

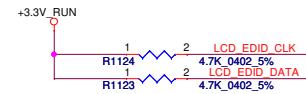
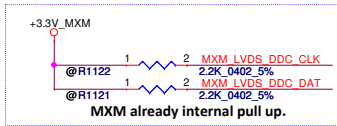
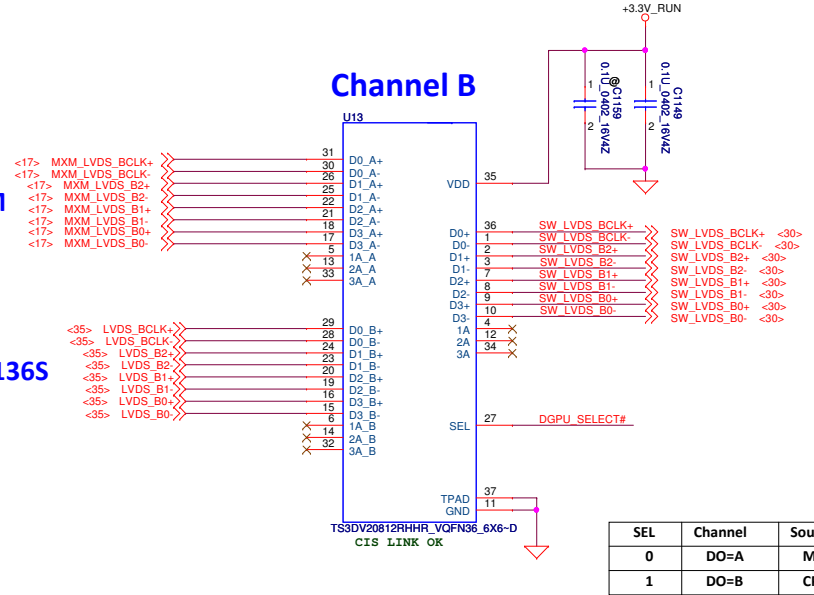
Channel A



From MXM

From RTD2136S

Channel B



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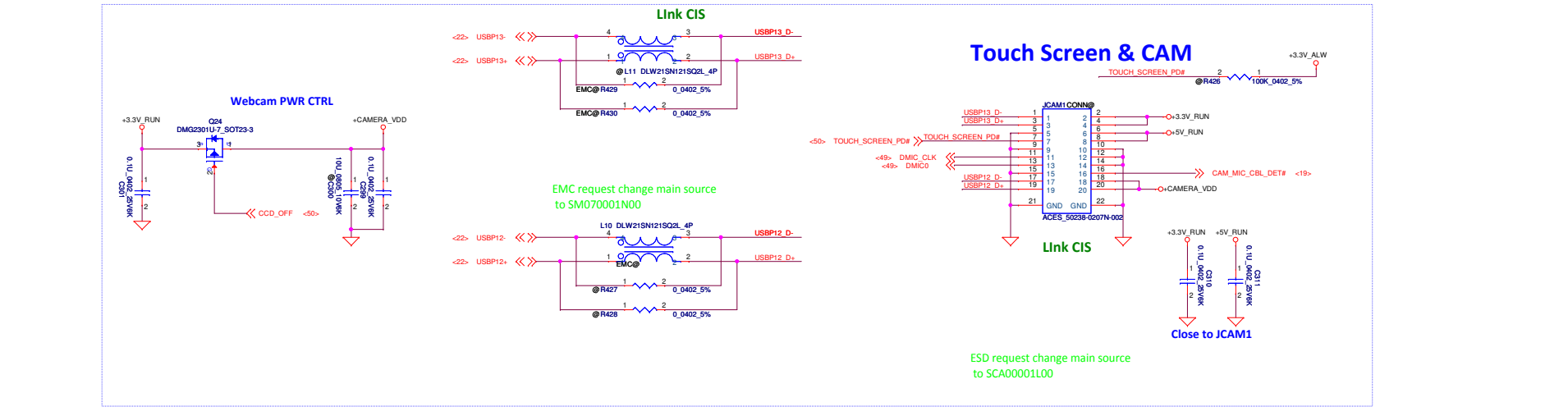
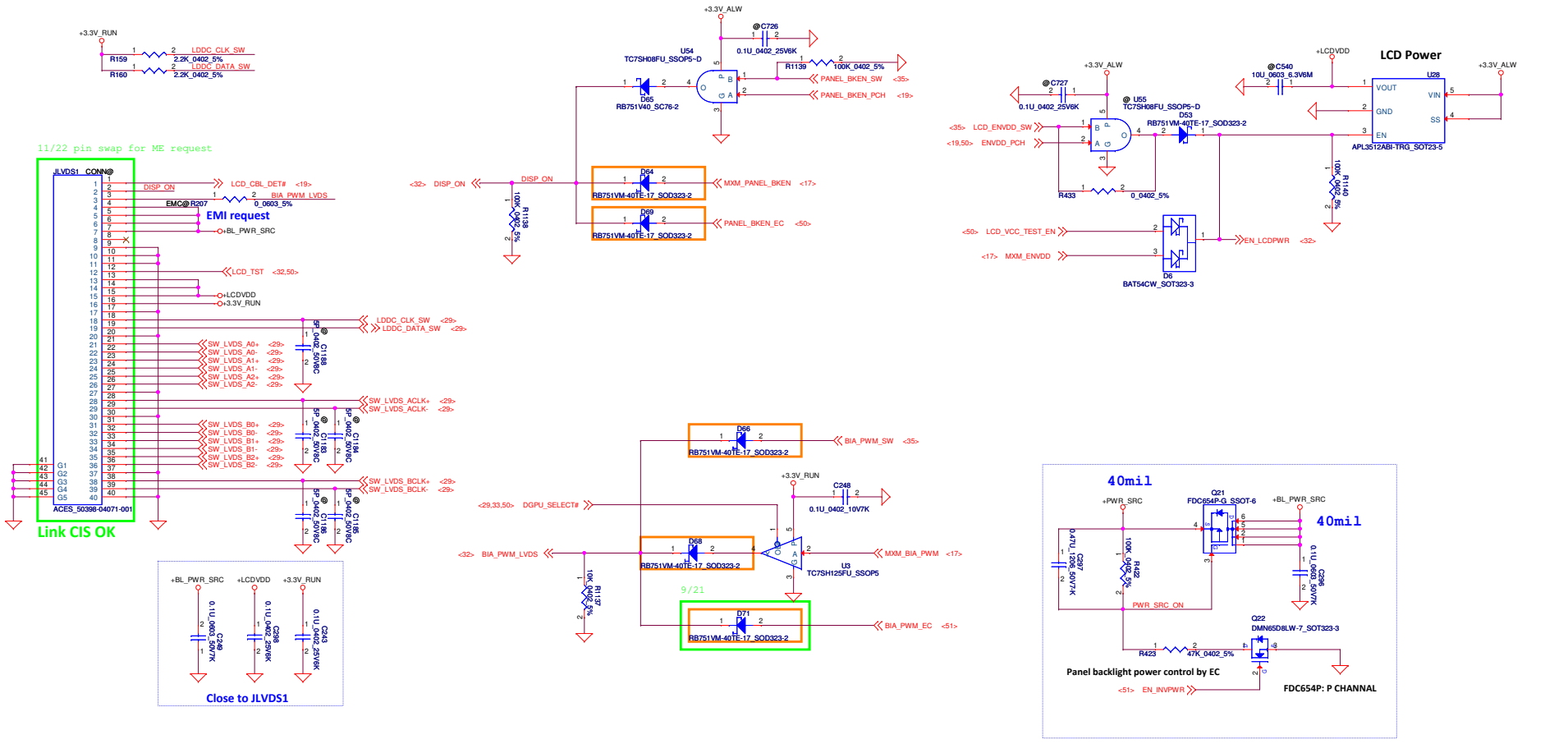
LVDS SW

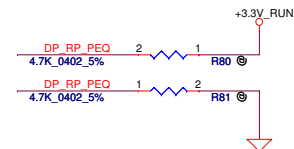
LA-9781P

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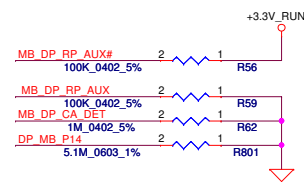
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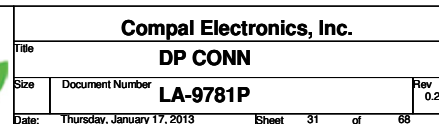




Programmable input equalization levels; Internal pull down at ~150k Ω , 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2
 H: HEQ, compensate channel loss up to 15dB @ HBR2
 M: LLEQ, compensate channel loss up to 5dB @ HBR2



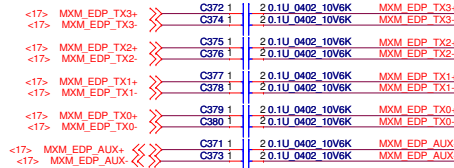
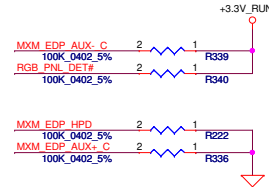
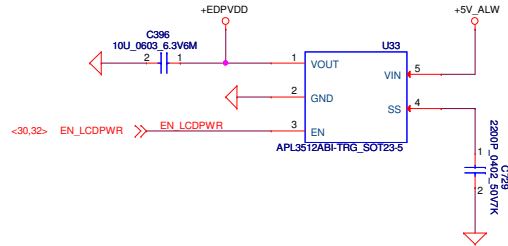
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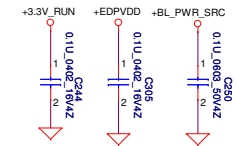
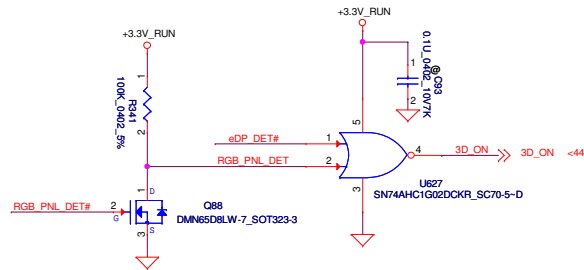
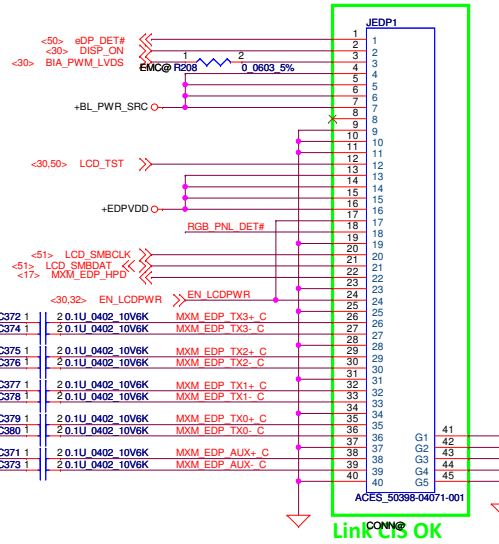
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EDP power



change eDP pin defined same as LVDS



Close to JEDP1

	EDP_DET#	RGB_DET#	3D_ON
RGB panel	0	1	0
3D panel	0	0	1
LVDS panel	1	0	0

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EDP CONN

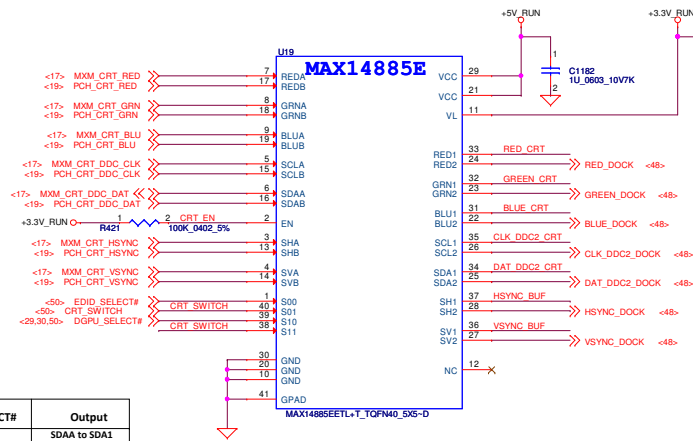
LA-9781P

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Channel A --> MXM

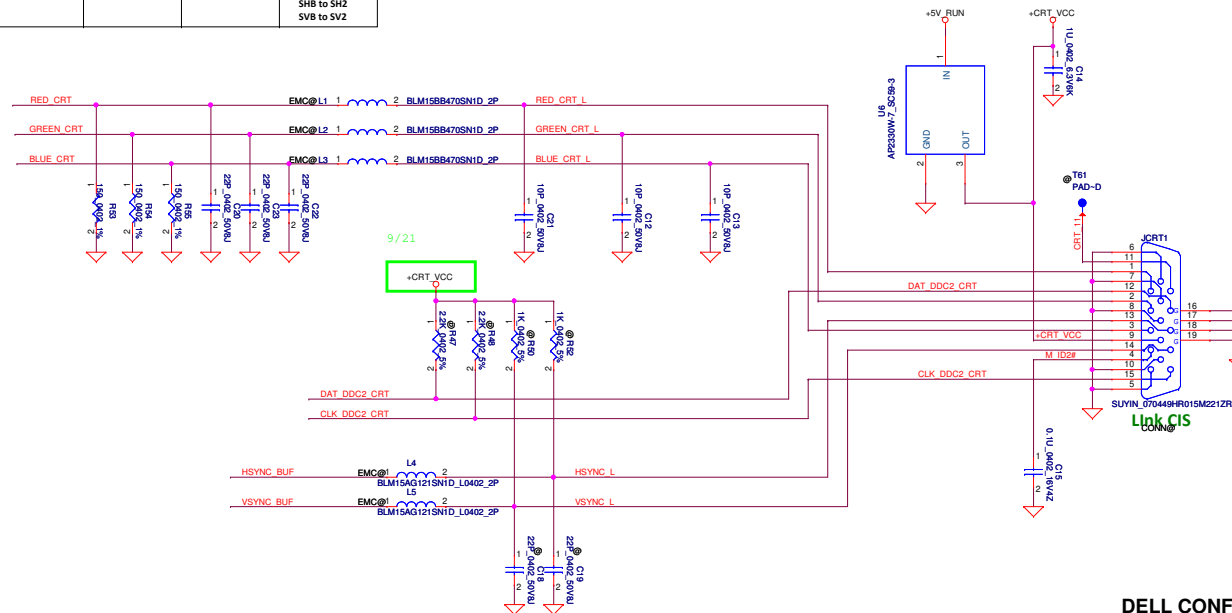
Channel B --> PCH



Port 1 --> MB board CRT

Port 2 --> Docking Port RGB

	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2



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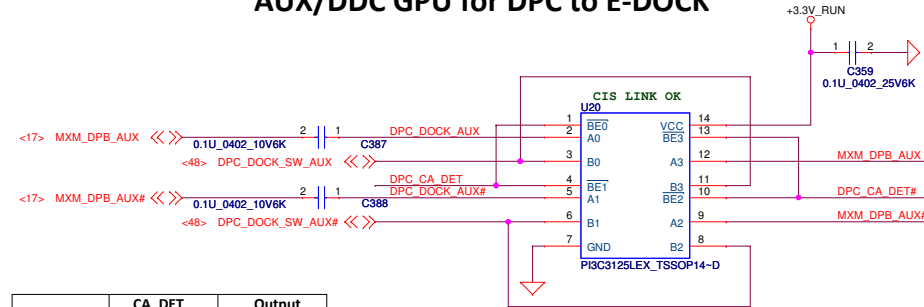
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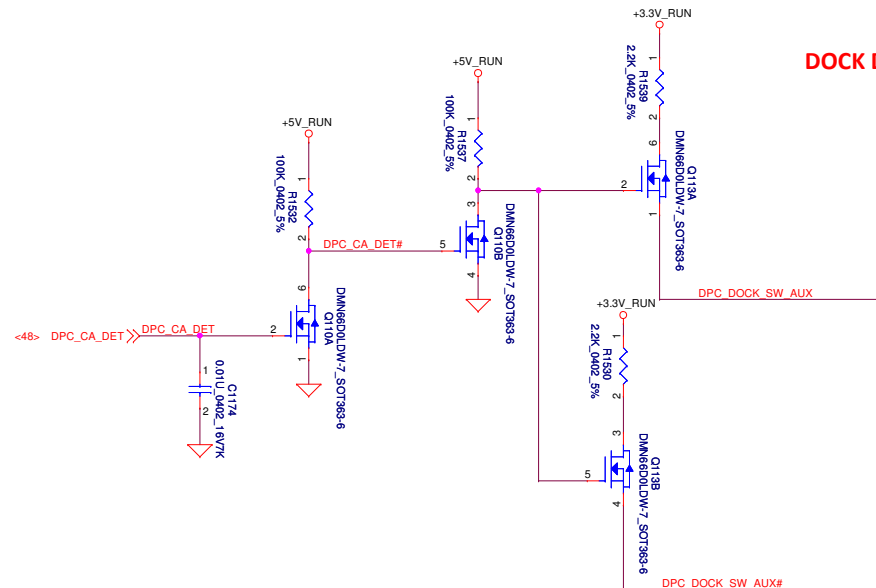
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AUX/DDC GPU for DPC to E-DOCK



	CA_DET	Output
HDMI/DVI	1	A2=B2 A3=B3
DP	0	A0=B0 A1=B1

DOCK DPB(PORT2) DDC



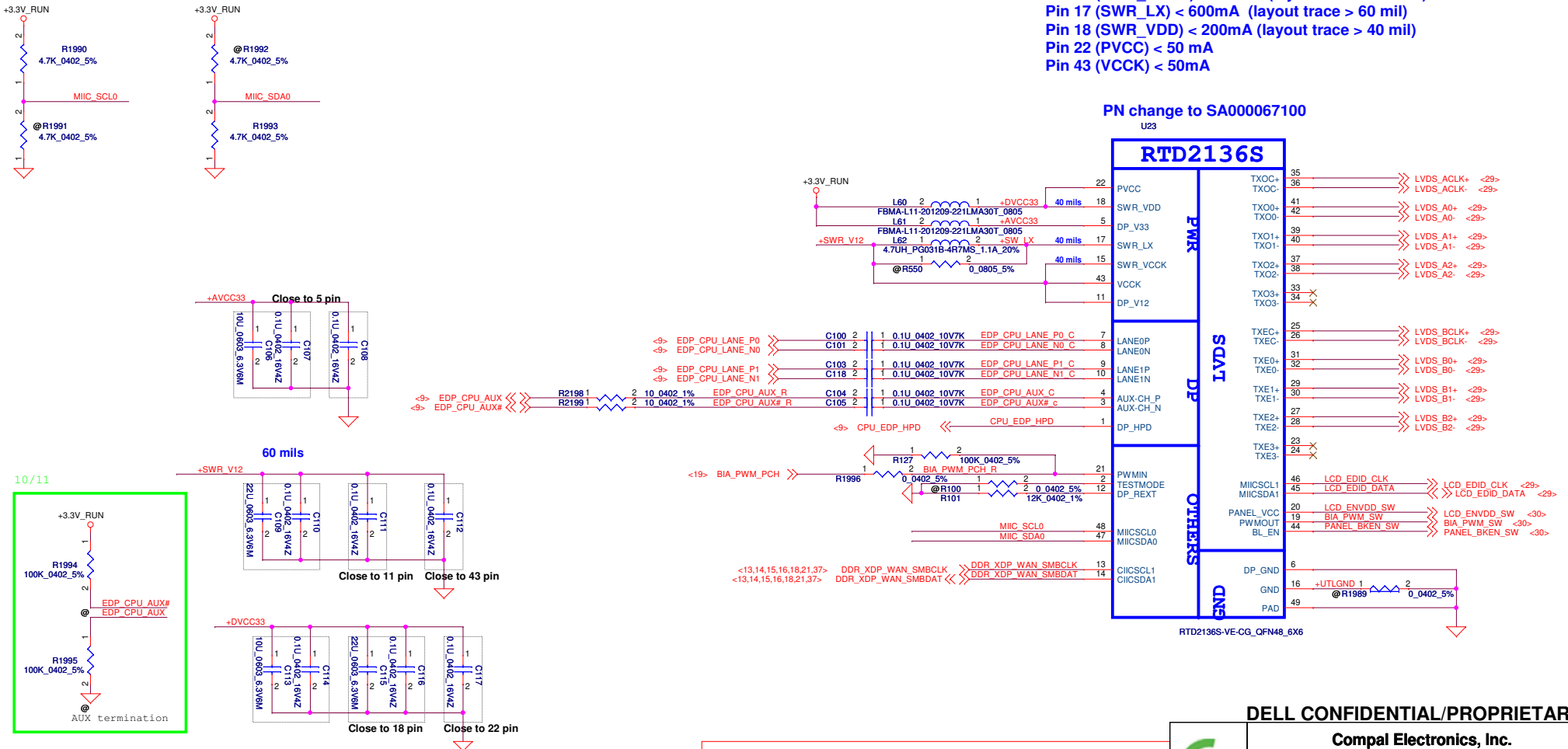
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Title	DP DDC SW		
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Power Consumption:
Pin 5 (DPV33) < 20mA
Pin 11 (DPV12) < 100mA
Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
Pin 22 (PVCC) < 50 mA
Pin 43 (VCCK) < 50mA

PN change to SA000067100

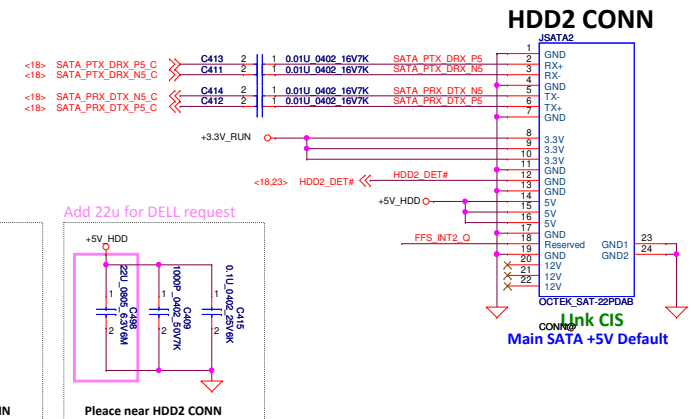
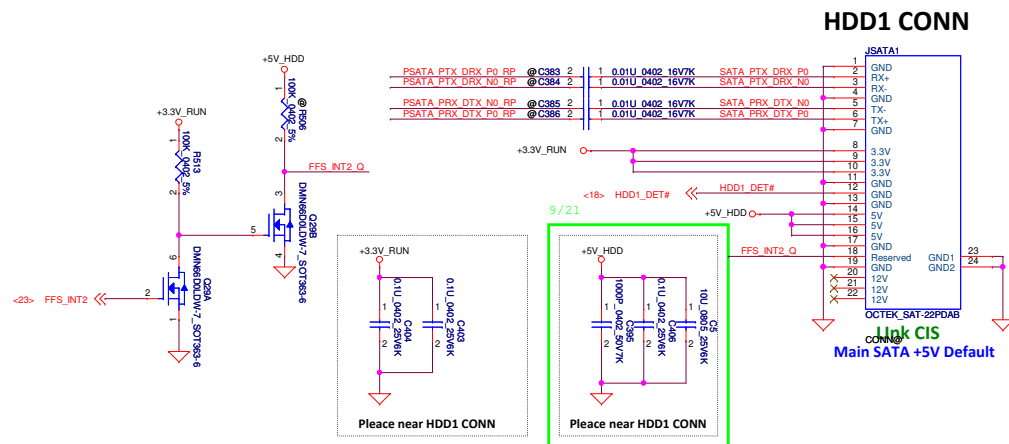
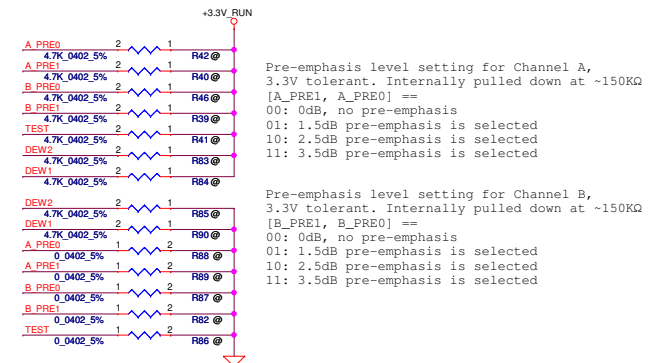
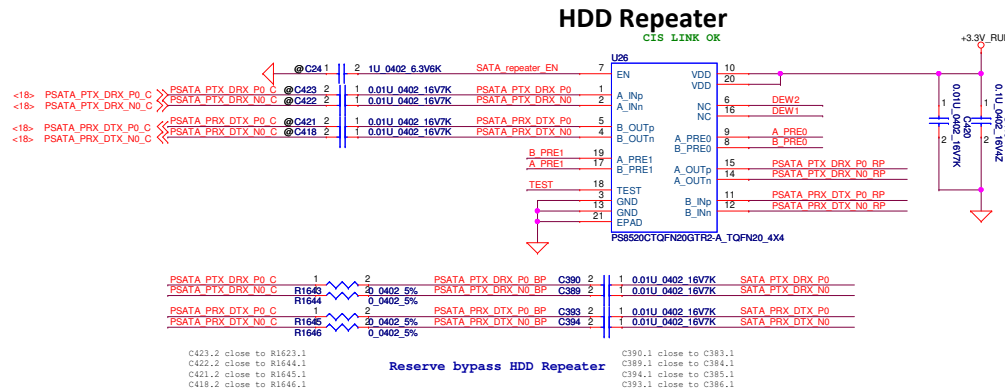
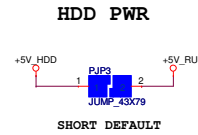


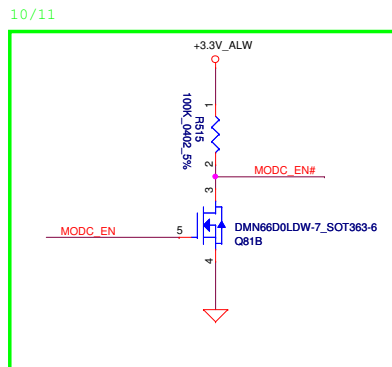
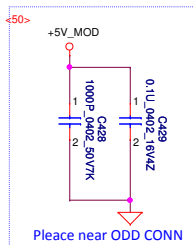
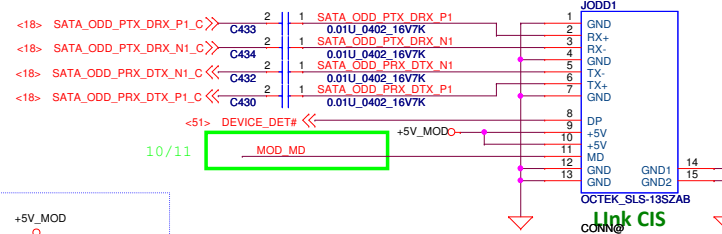
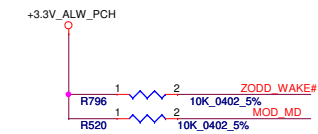
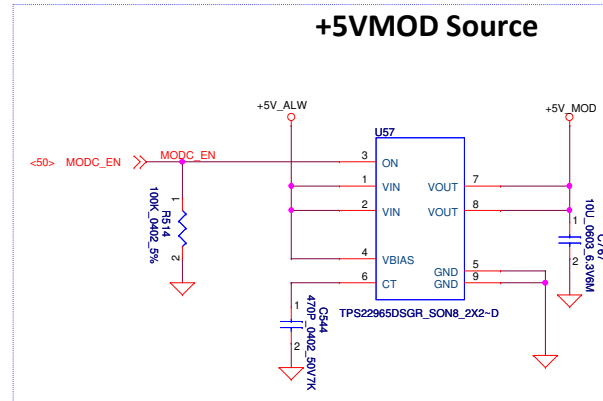
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Title			
eDP to LVDS			
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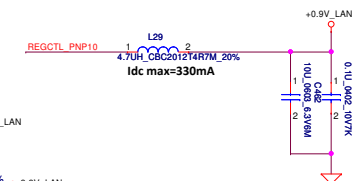
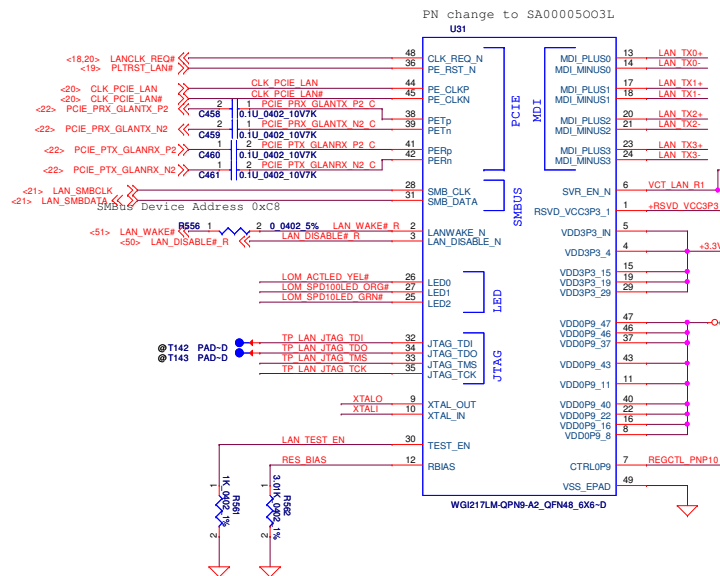
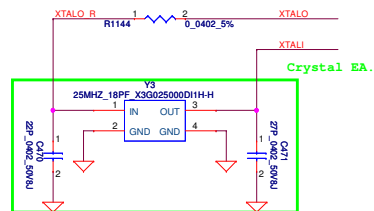
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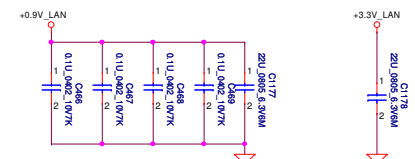


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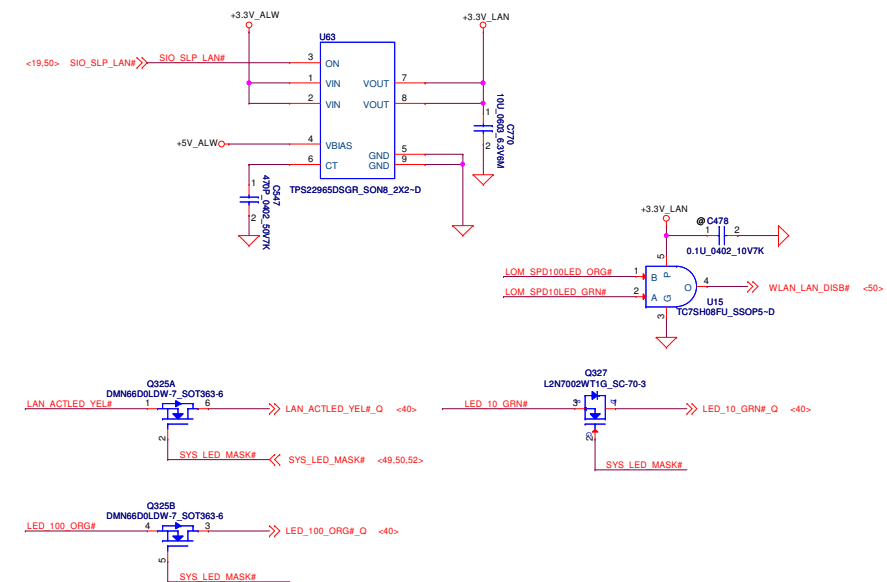
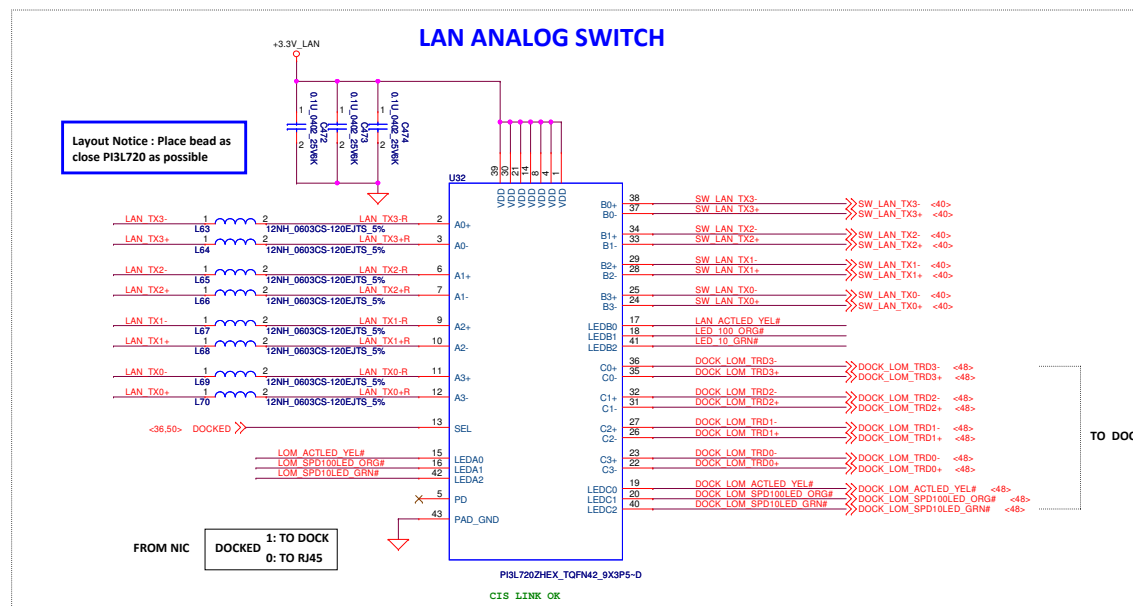
Place R548, C462, C463 and L29 close to U31



Note: +1.0V_LAN will work at 0.95V to 1.15V

Place C1178 close to pin5

+1.0V_LAN POWER OPTIONS	
Shared with PCH 1.05V SVR	* Internal SRV
STUFF: R548 NO STUFF: L29	STUFF: L29 NO STUFF: R548



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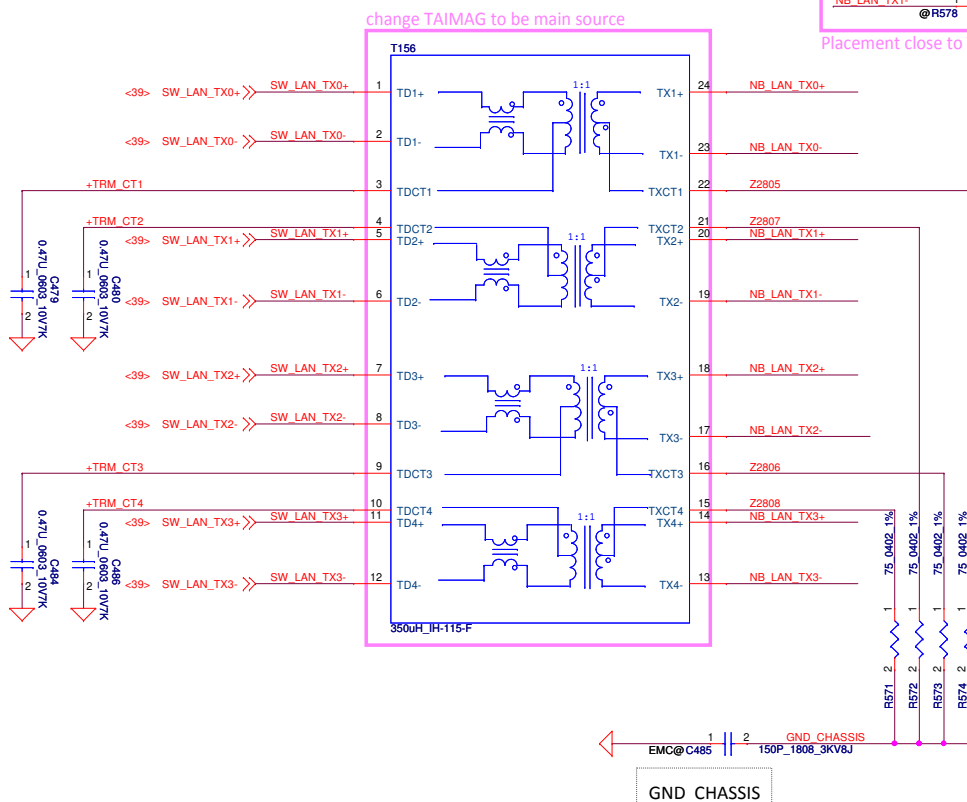
Compal Electronics, Inc.

LAN/LAN SW

LA-9781P

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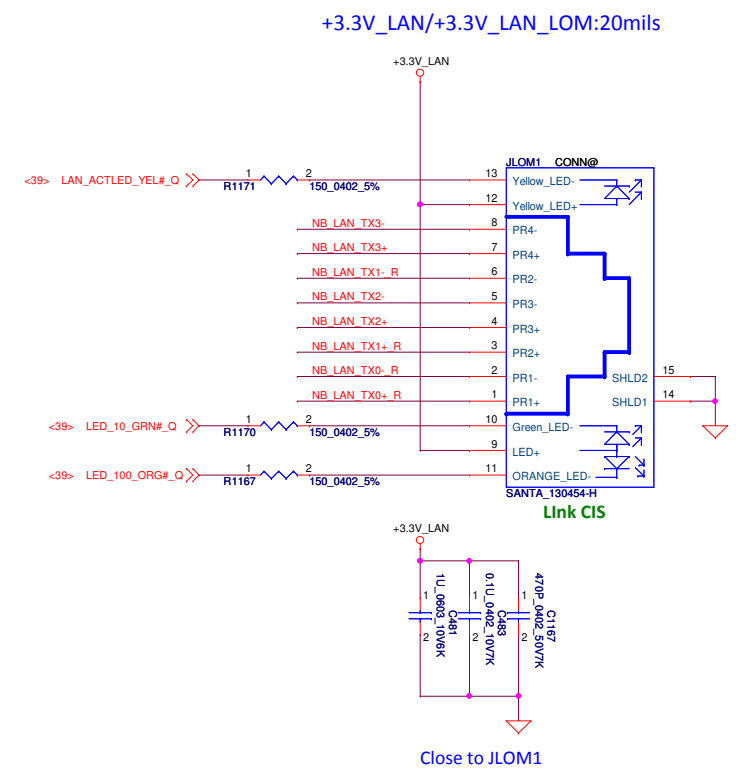
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For IEEE EA request

NB_LAN_TX0+	@R575	0.0402_5%	NB_LAN_TX0+ R
NB_LAN_TX0-	@R576	0.0402_5%	NB_LAN_TX0- R
NB_LAN_TX1+	@R577	0.0402_5%	NB_LAN_TX1+ R
NB_LAN_TX1-	@R578	0.0402_5%	NB_LAN_TX1- R

Placement close to T156

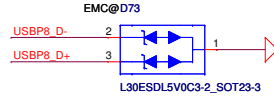
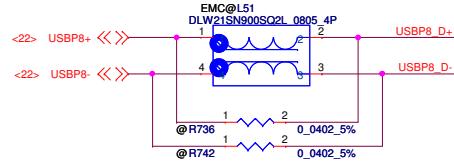


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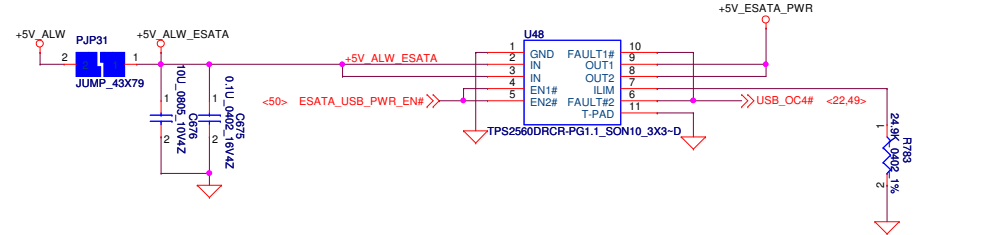
Compal Electronics, Inc.			
RJ45			
Size	Document Number	LA-9781P	Rev 0.2
Date:	Thursday, January 17, 2013	Sheet 40	of 68

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EMC request change main source
to SM070001N00

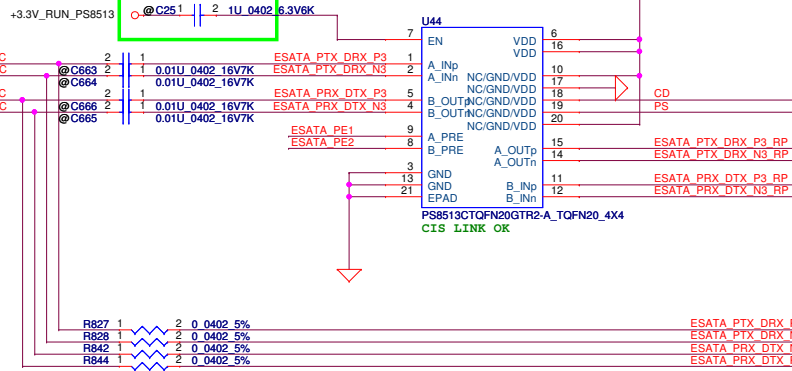


ESD request change main source
to SCA00001L00

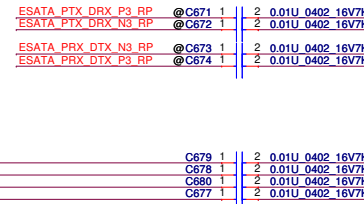
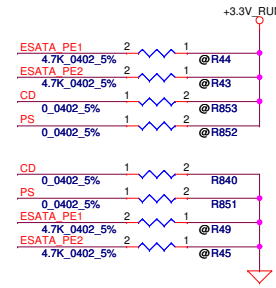


ESATA Repeater

9/27



C663.2 close to R827.1
C664.2 close to R828.1
C665.2 close to R842.1
C666.2 close to R844.1



C679.2 close to C671.2
C678.2 close to C672.2
C680.2 close to C673.2
C677.2 close to C674.2

Reserve bypass ESATA Repeater

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ESATA

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Rev 0.2

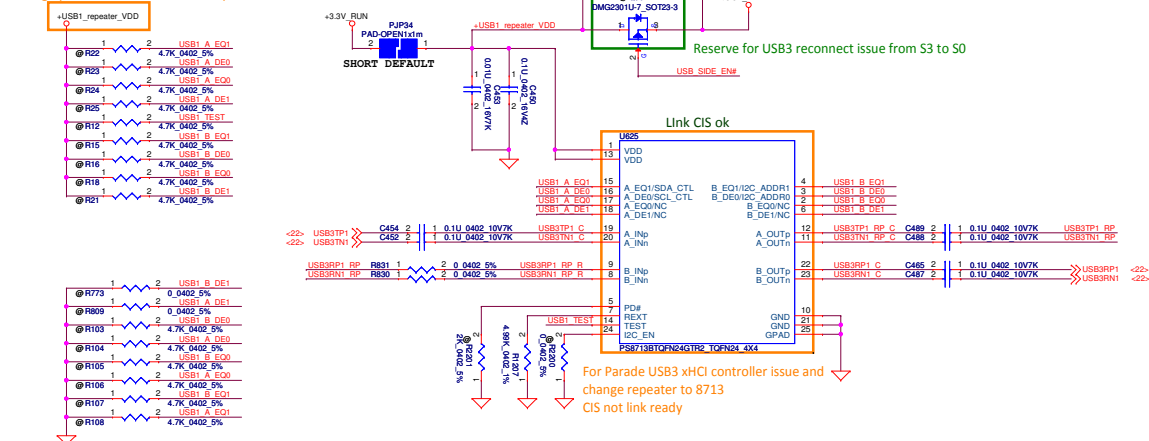
Date: Thursday, January 17, 2013

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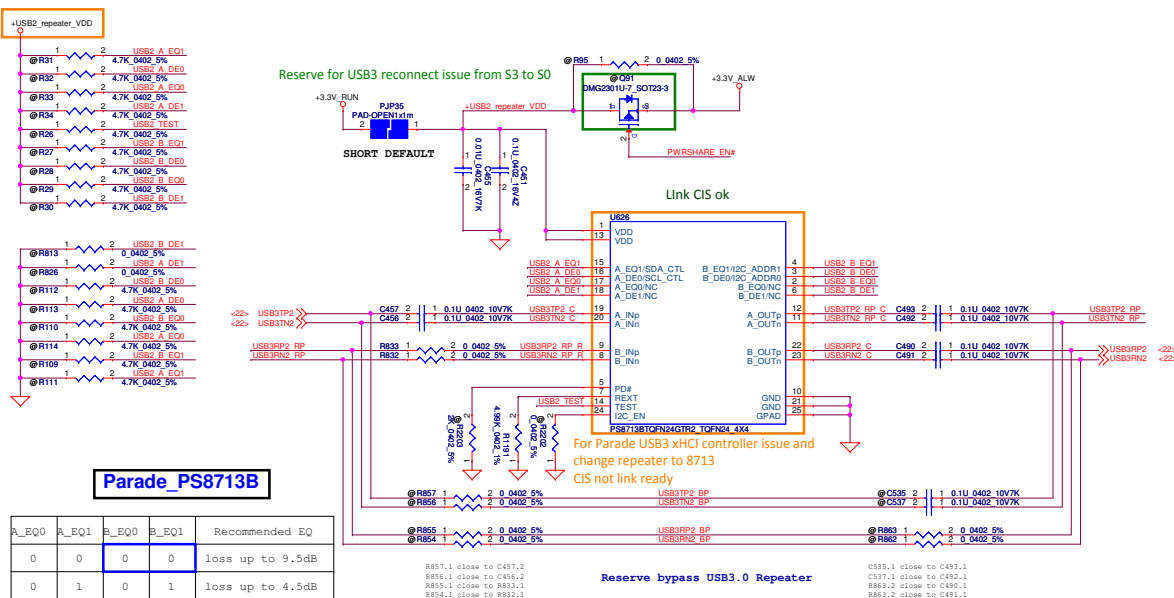
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Change power net to meet USB1 repeater VDD



Change power net to meet USB2 repeater VDD

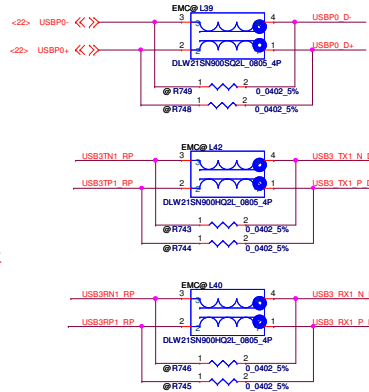


A_EQ0	A_EQ1	B_EQ0	B_EQ1	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 4.5dB
1	0	1	0	loss up to 13dB
1	1	1	1	loss up to 7.5dB

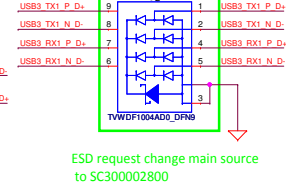
Both A_EQ0&B_EQ have internal pull-down 150k

Reserve bypass USB3.0 Repeater

EMC request change main source to SM070001N00



For ESD request



ESD request change main source to SCA00001L00



Power share SW

change SILEGO to be main source

PN change to SA00006L600, wait symbol release.

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

EMC request change main source to SM070001N00

For SILEGO power share SW EA

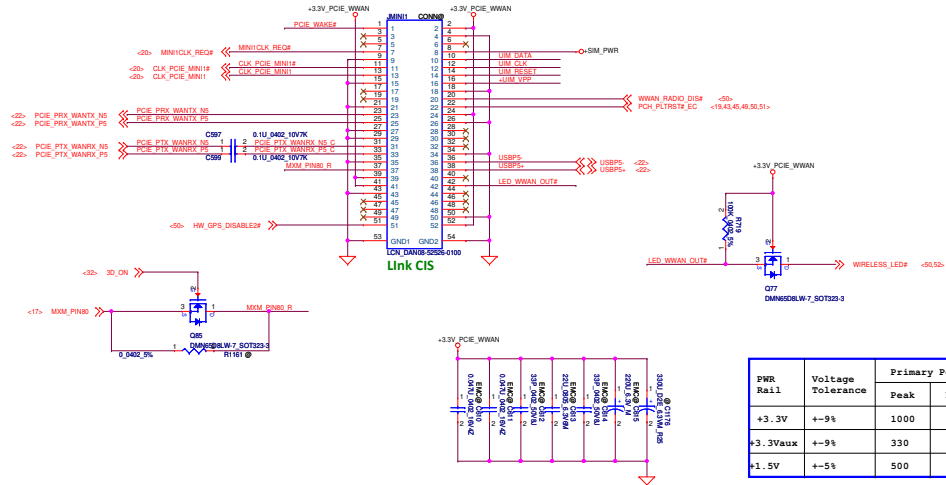
EMC request change main source to SM070001N00

For SILEGO power share SW EA

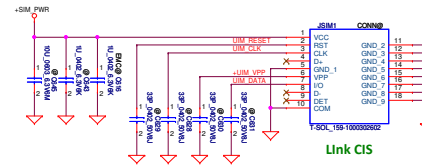
EMC request change main source to SM070001N00

For SILEGO power share SW EA

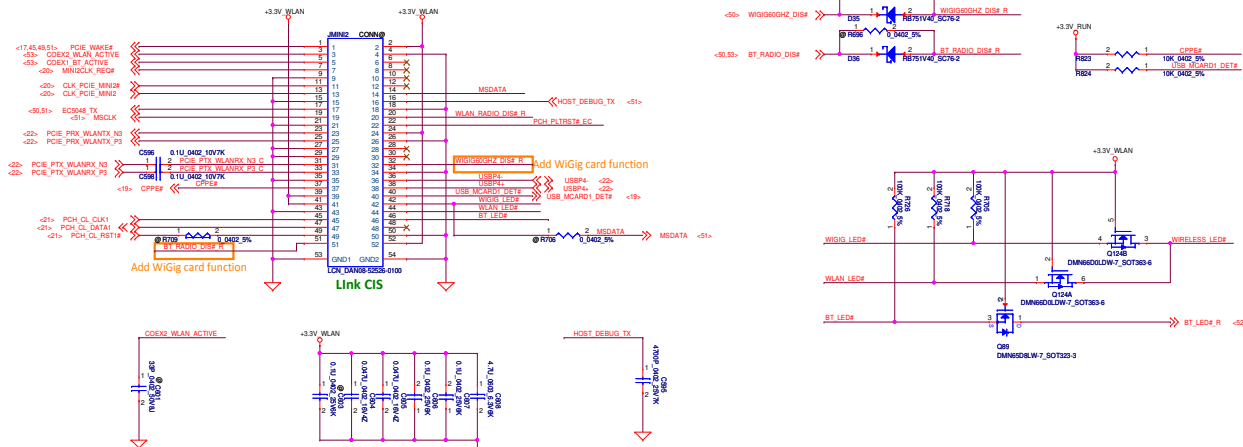
Mini WWAN/GPS/LTE H= 4 mm



SIM Card Push-Push type



Mini WLAN/WiMAX/WiGig H=5.2



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Mini Card-1/2

LA-9781P

Rev 6.2

The schematic diagram illustrates the electrical connections for a PCIE flash and a PCIE controller. The top section shows the PCIE flash (LON_DAN08-52526-0100) connected to a +3.3V_VCC1_FLASH supply. The bottom section shows the PCIE controller (Link C15) connected to a +3.3V_VCC2_FLASH supply. The schematic includes various signal lines such as MIN3CLK_REQ#, CLK_PCIE_MINI3#, and PCIE_PTX_WPANRX_N# and PCIE_PTX_WPANRX_P#.

The diagram illustrates the internal wiring of a SATA-to-PCIe adapter. It shows the connection between the SATA connector (pins 1-50) and the SATA controller (C447, C448, C445, C446). The SATA controller is connected to the SATA-to-PCIe bridge (C447, C448), which is then connected to the PCIe controller (C447, C448). The diagram also shows the power supply connections for the SATA and PCIe interfaces, including the 3.3V and 5V pins.

Legend:

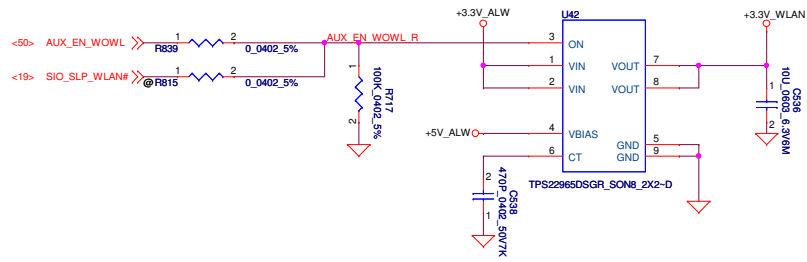
- "LOW"=SATA; "HIGH"=PCIe
- Check Samsung SSD card
- Insert card, pin51=low
- Pull out card, pin51=high

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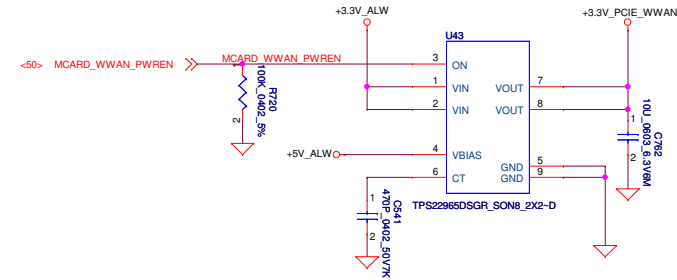
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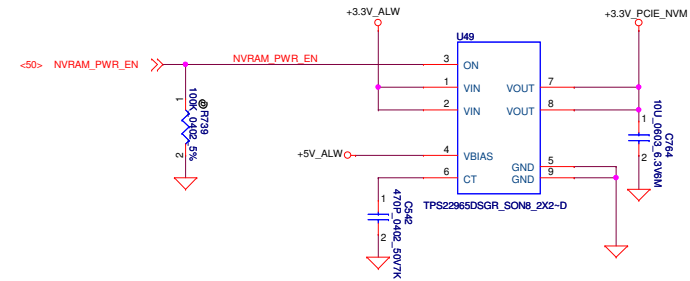
Power Control for Mini card2



Power Control for Mini card1



Power Control for Mini card4



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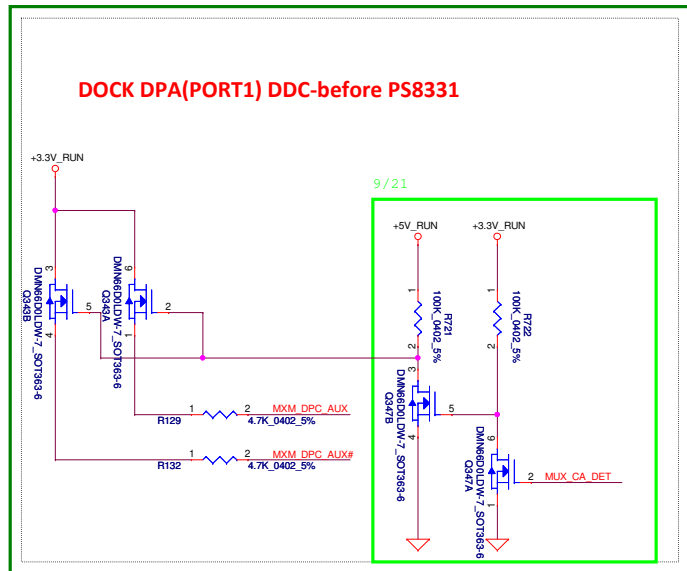
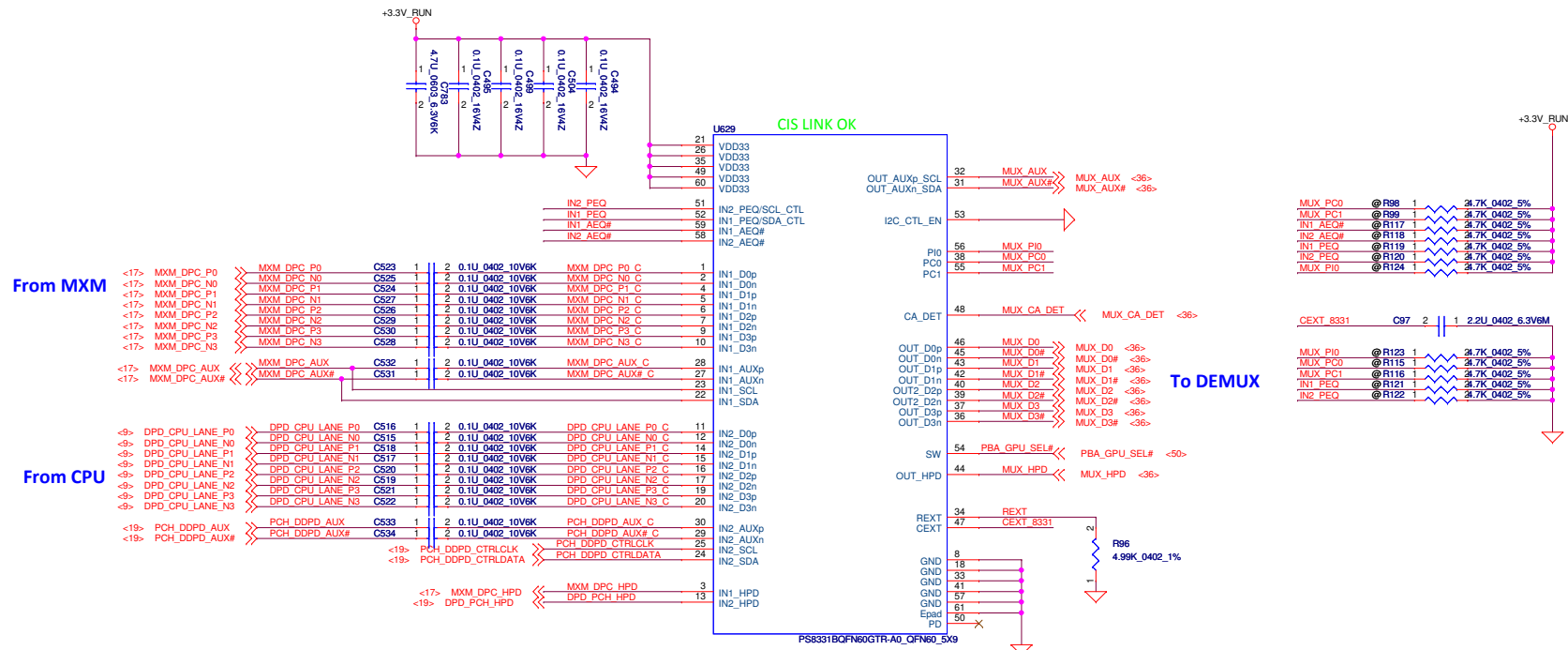
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Mini Card PWR

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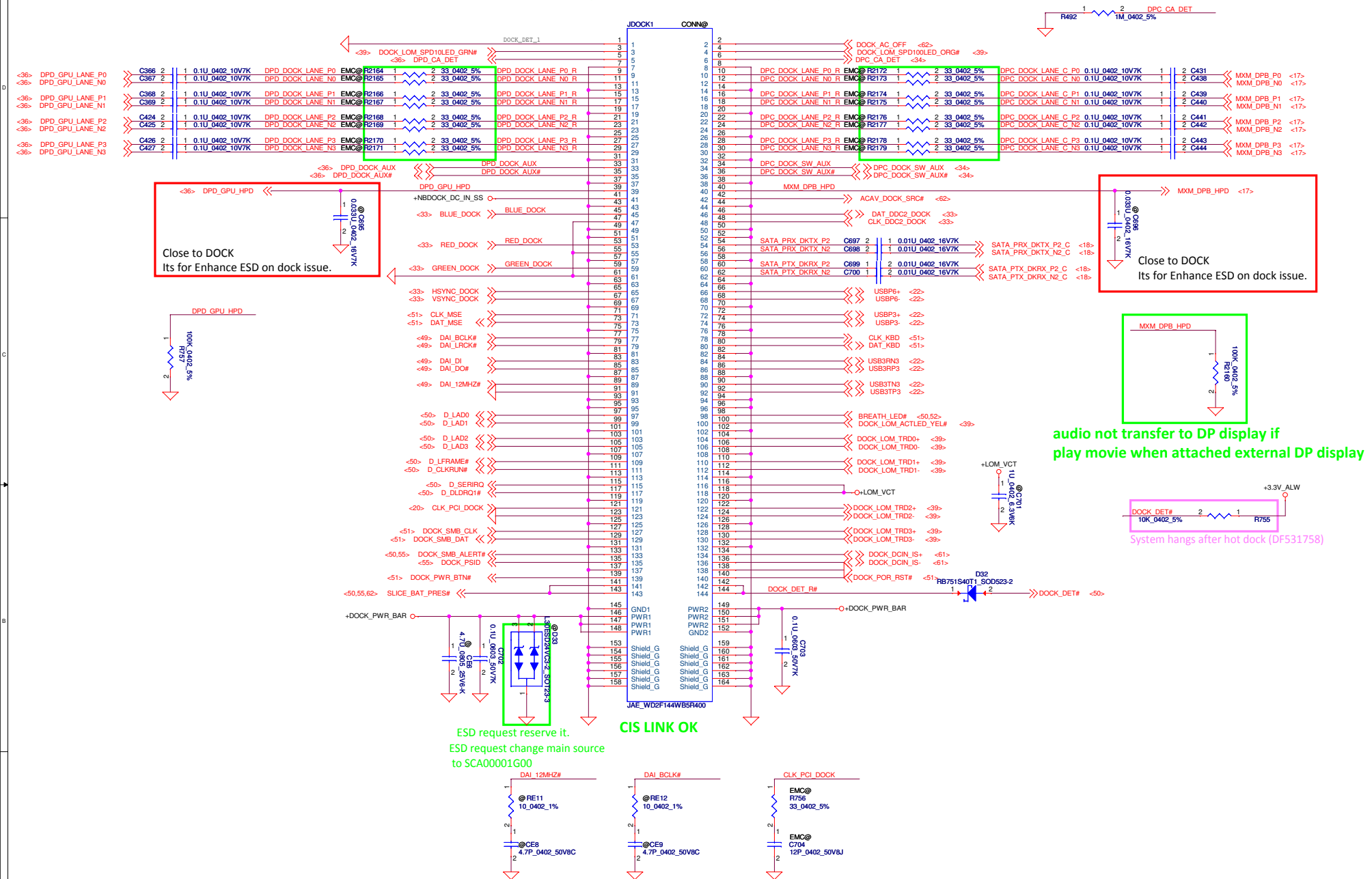
MXM/CPU MUX(PS8331)

File
Size
Document Number
LA-9781P
Rev
0.2
Date
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EMI request add 33ohm for DOCK DVI signals.



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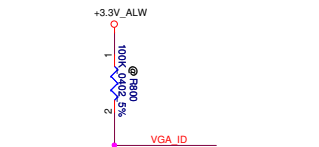
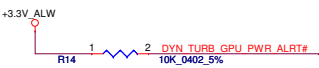
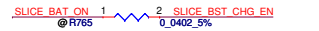
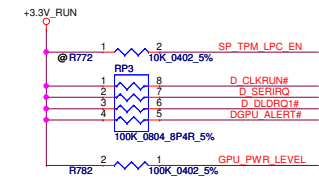
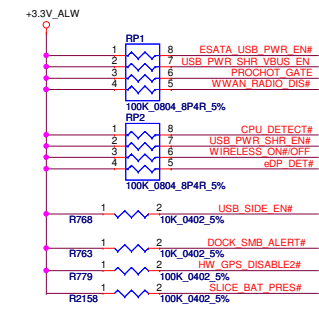
Docking

LA-9781P

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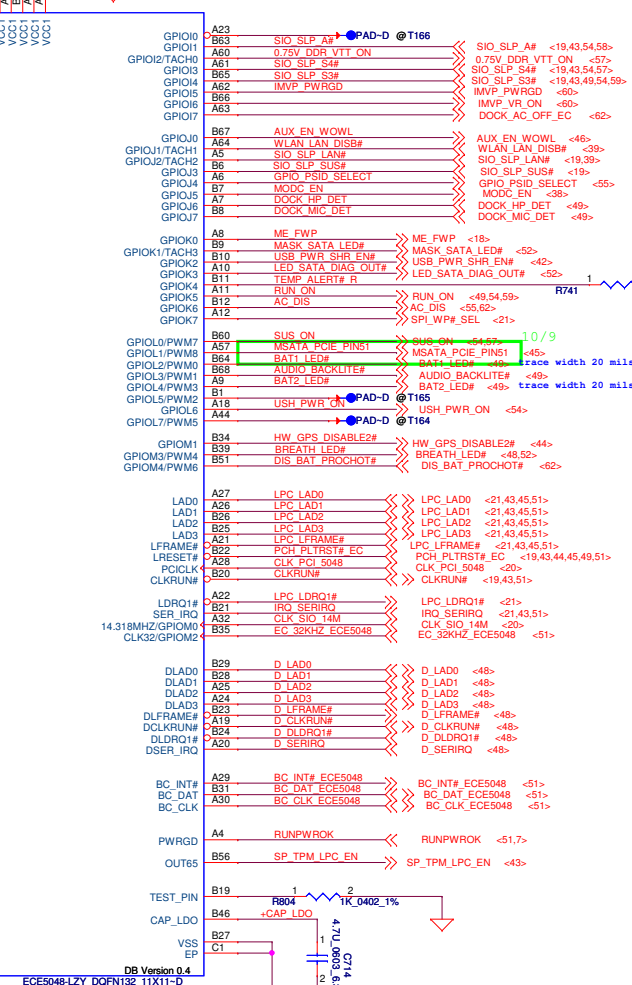
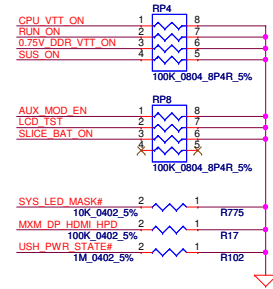
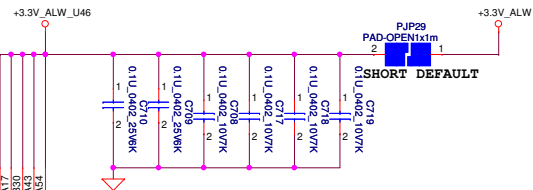
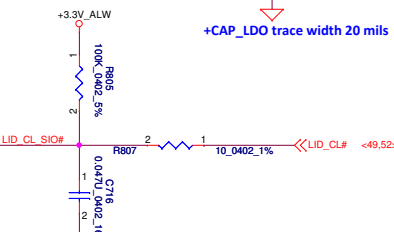
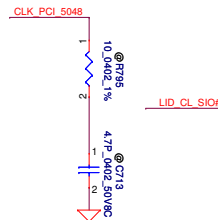
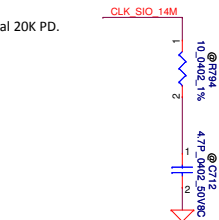
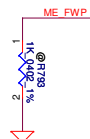
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	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)



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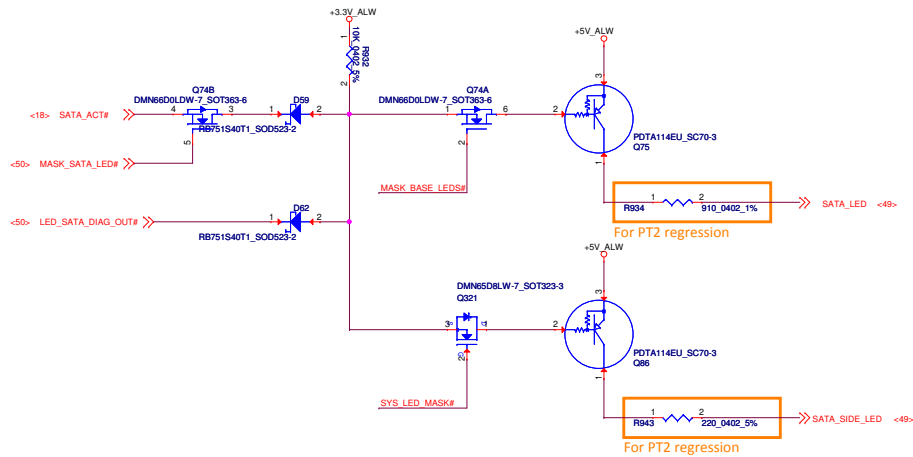
SIO

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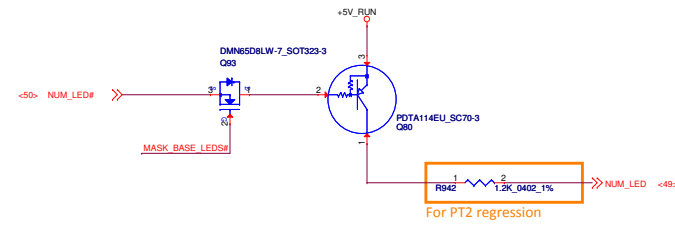
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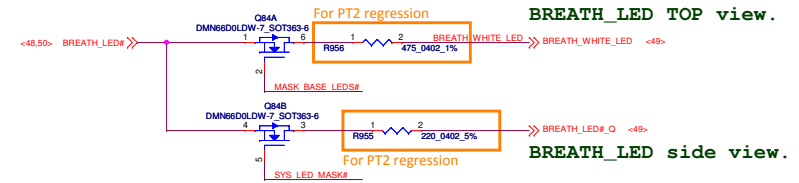
HDD LED



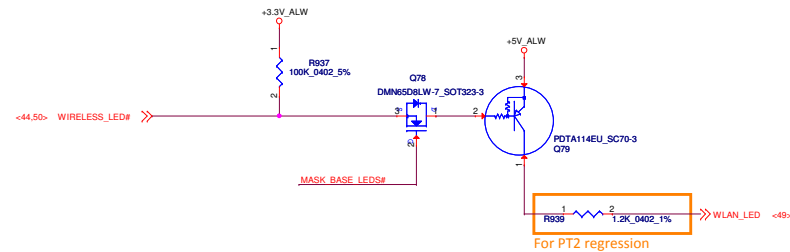
NUM LED



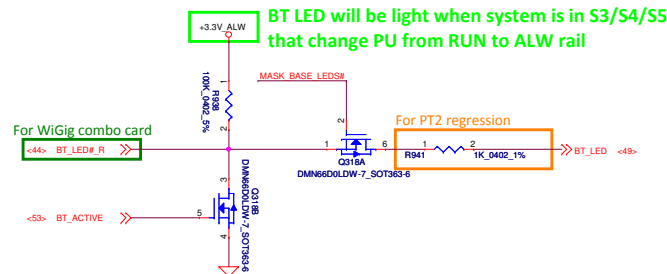
Breath LED



WWAN/WLAN LED



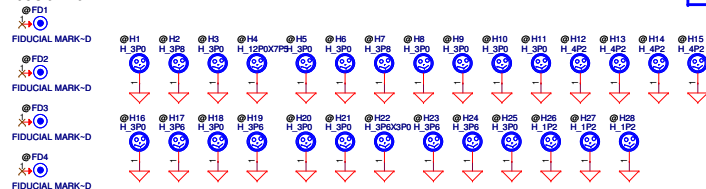
BT LED



LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

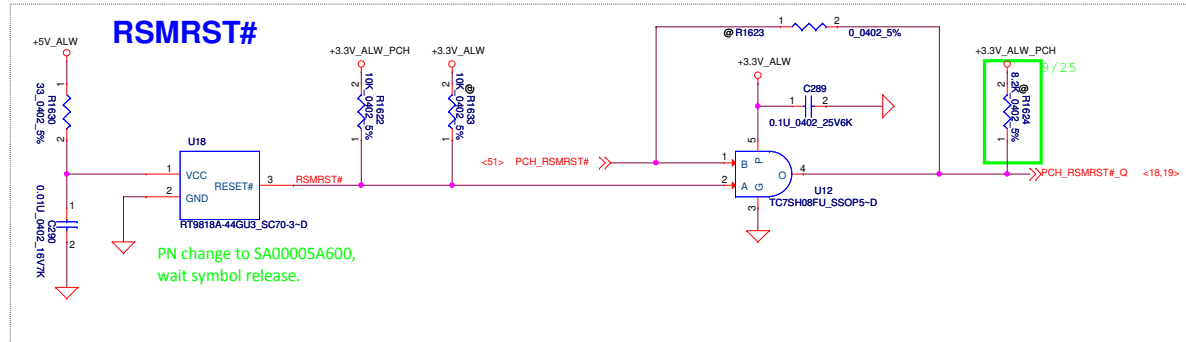


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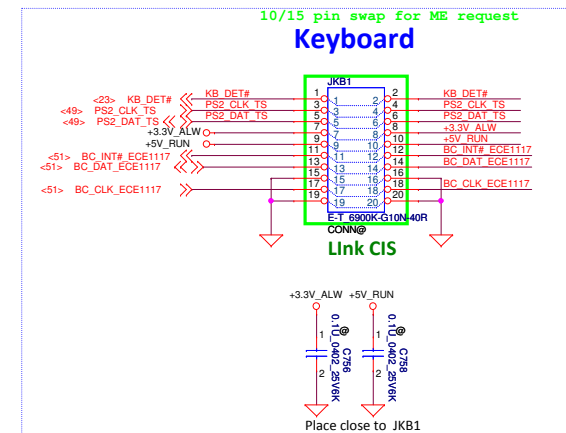
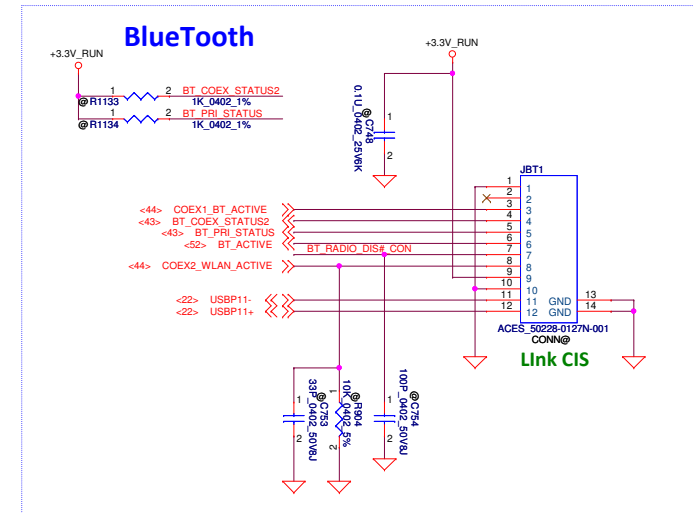
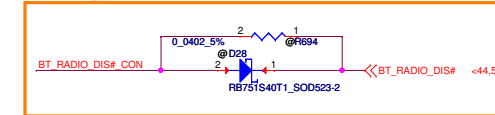
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PAD & Standoff & LED

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Add WiGig card function



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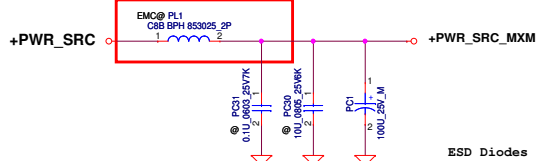
Touch PAD/Int KB

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Rev 0.2

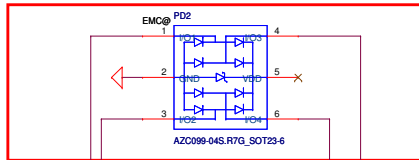
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EMI Part (35.33)

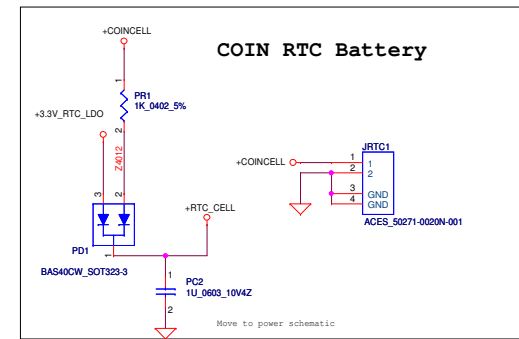
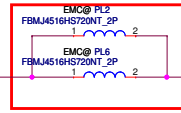


ESD Diodes

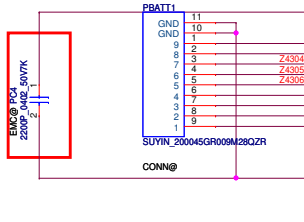
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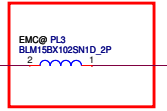
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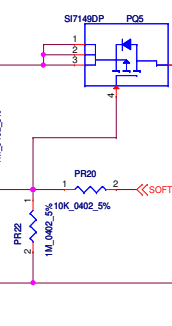
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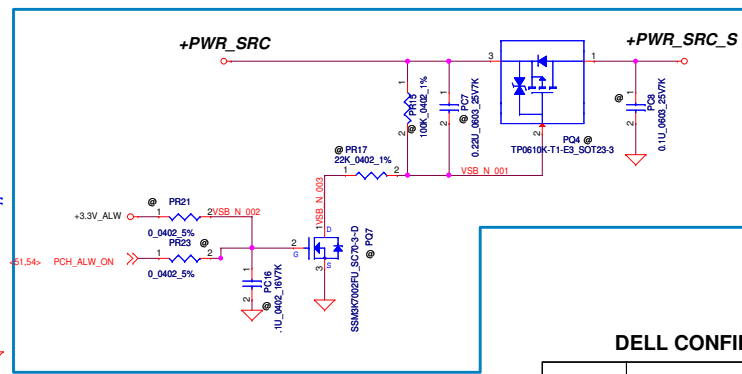
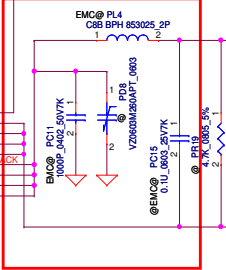
EMI Part (35.33)



DC_IN+ Source



EMI Part (35.33)



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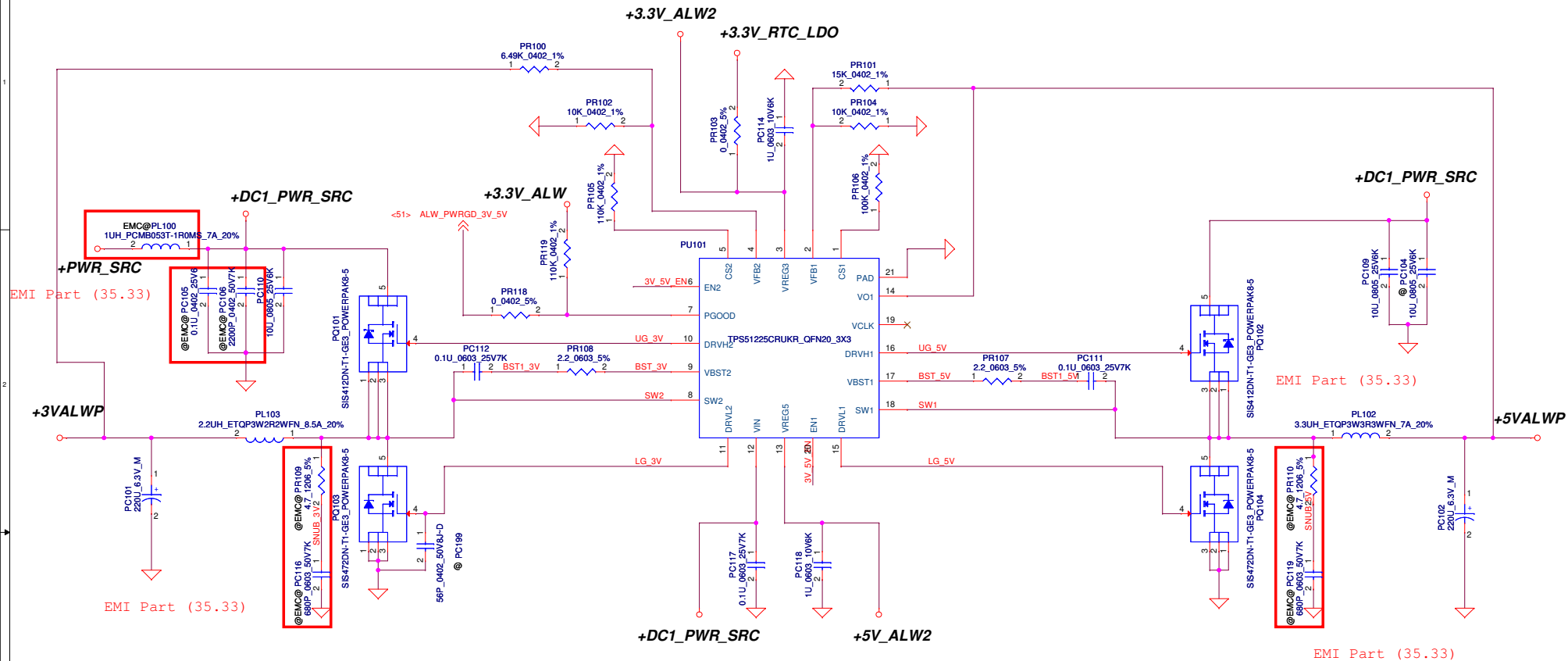
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+DCIN

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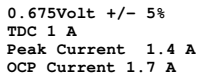
3VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 350kHz
TDC 6.1 A
Peak Current 8.7 A
OCP current 10.5 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	10.3mohm	12.4mohm
Choke DCR Max	17mohm	
Choke Ityp	8.3A	10.8A
Bulk cap ESR	15mohm	

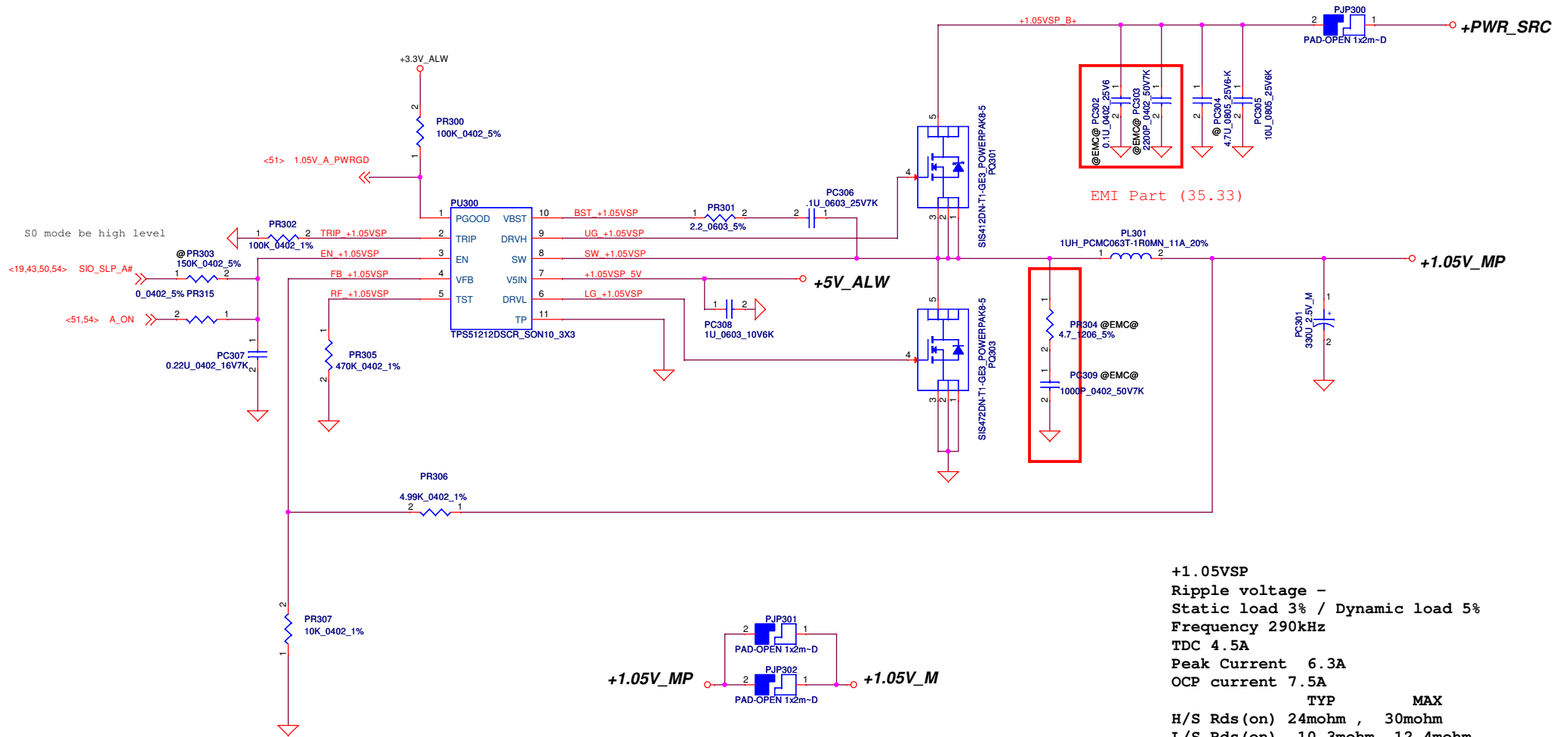
5VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 300kHz
TDC 6 A
Peak Current 8.5 A
OCP current 10.2 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	10.3mohm	12.4mohm
Choke DCR Max	28mohm	
Choke Ityp	6.6A	8.2A
Bulk cap ESR	15mohm	

Security Classification		Compal Secret Data		Title	
Issued Date	2012/01/17	Deciphered Date	2013/01/16	PWR-3VALWP/SVALWP	
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+1.05VSP

Ripple voltage -

Static load 3% / Dynamic load 5%

Frequency 290kHz

TDC 4.5A

Peak Current 6.3A

OCP current 7.5A

TYP MAX

H/S Rds(on) 24mohm , 30mohm

L/S Rds(on) 10.3mohm , 12.4mohm

Choke DCR 11mohm

Choke Ityp:11A / Isat:14.5A

Bulk cap ESR 17mohm

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Iada=0~12.3A(240W)

$$ADP_I = 40 \times I_{\text{adapter}} \times R_{\text{sense}}$$

+PWR_SRC

EMC@ PL700

1UH_PCB053T-1R0MS_7A_20%

+CHARGER_SRC

CC = 3.52A (Normal)

CV = 13.3V

VIN in detect limit

$$+SDC_IN = 2.4V / 82.5 \times (82.5 + 499) = 16.9V$$

Current limit
Charger :8A V_{lim}=1.6V :
Max Boost Charger 12A V_{lim}=2.4V
9 Cell (1.3C)

Maximum charging current is 7.2A

DYN_TUR_CURRENT_SET#	
210W	High
240W	Low

Adapter Protection Circuit for Turbo Mode

Security Classification

Issued Date

2012/01/17

Compal Secret Data

Deciphered Date

2013/01/16

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Title

PWR-Charger

Size

Document Number

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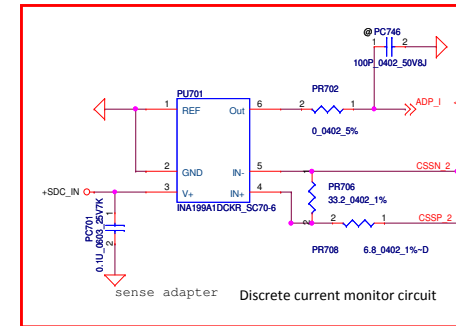
Rev

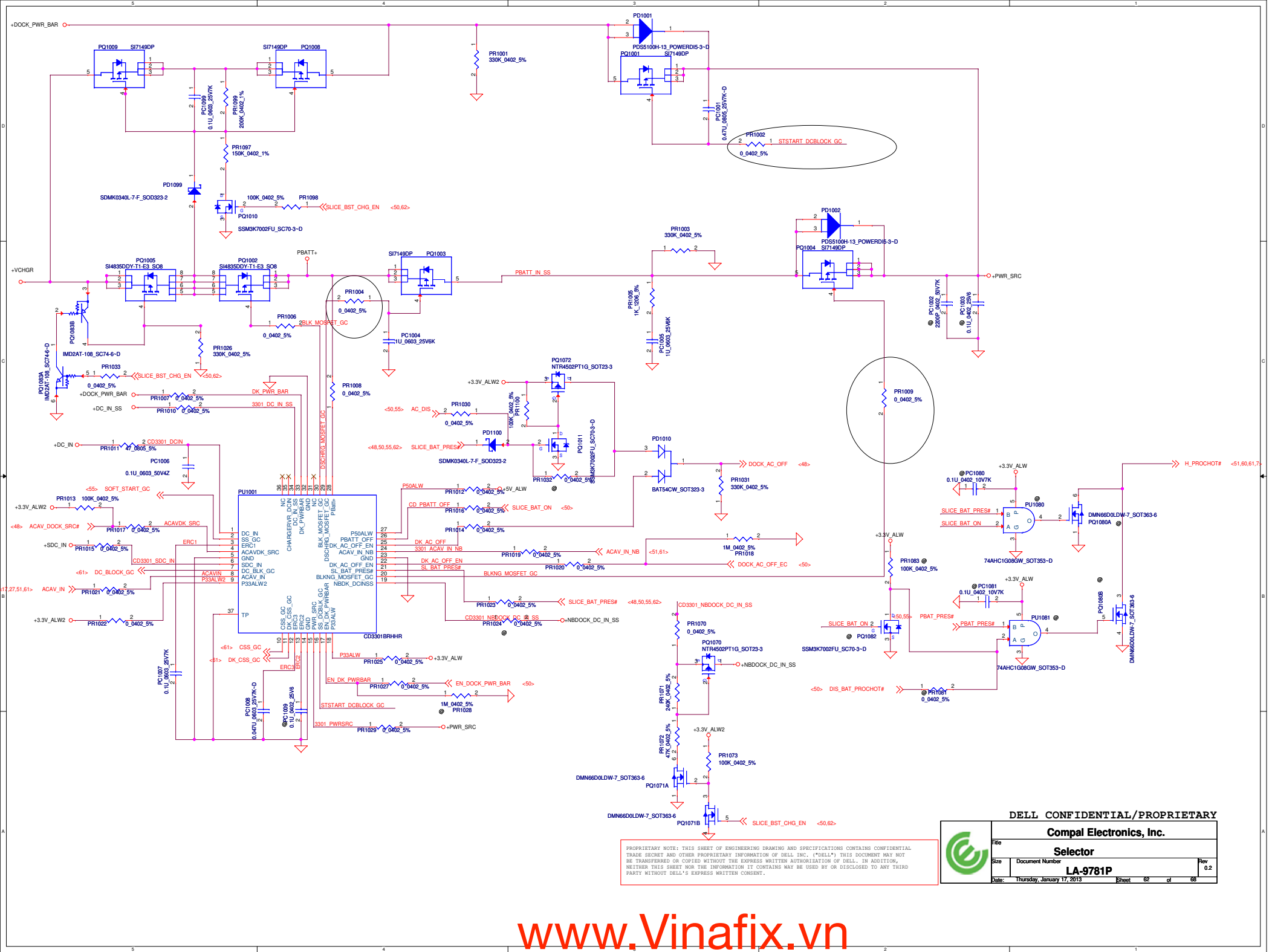
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Date: Thursday, January 17, 2013

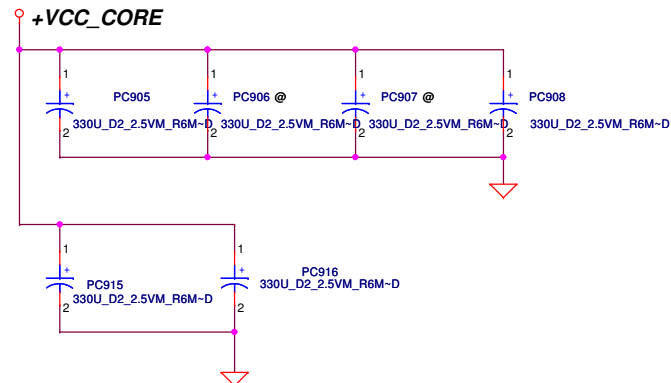
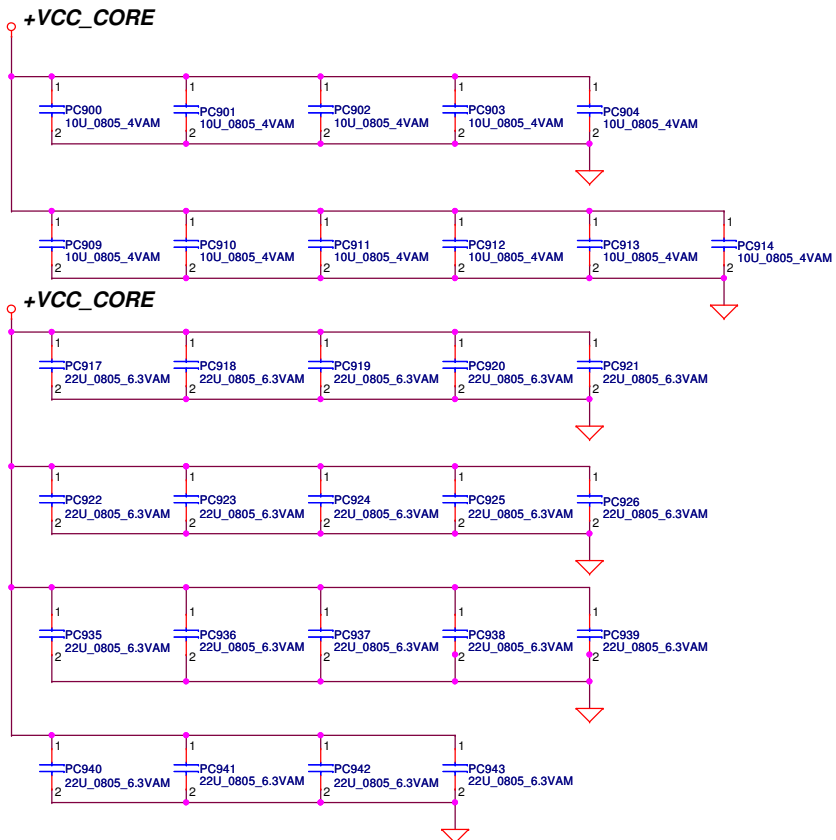
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Based on PDDG rev 0.7 Table 5-1.



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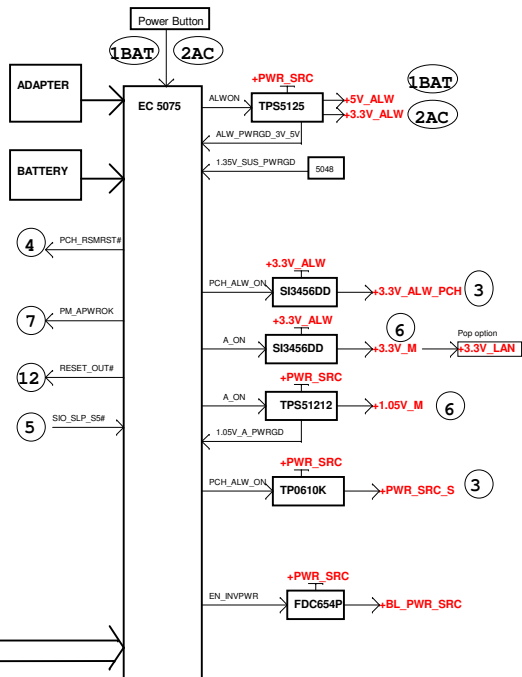
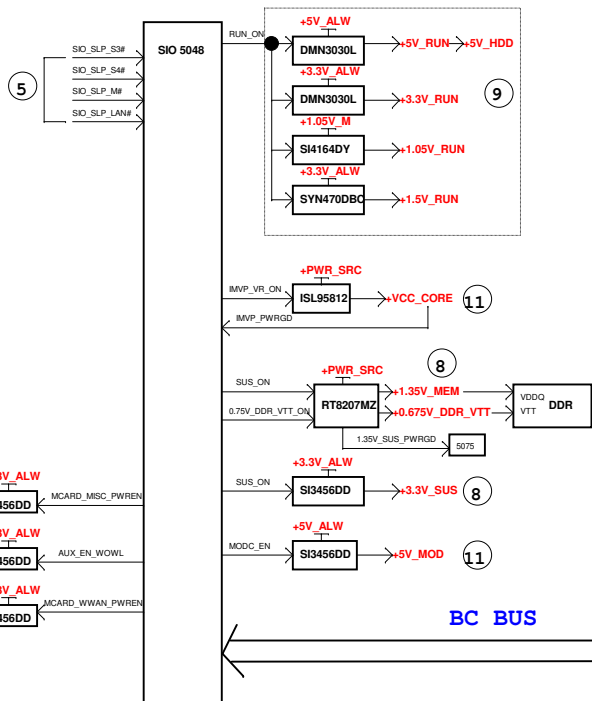
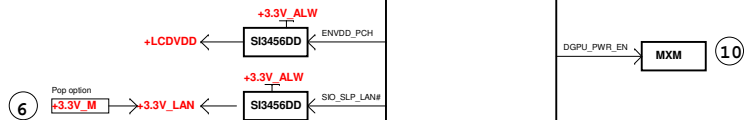
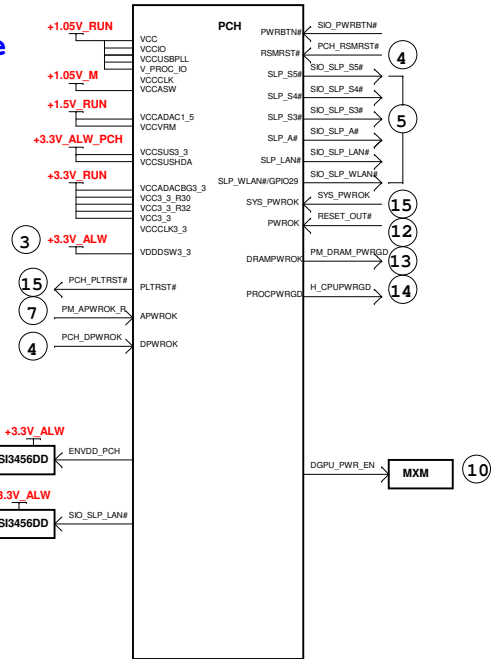
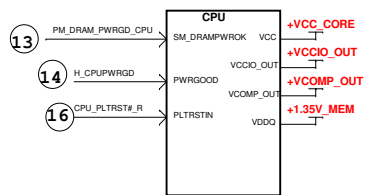
PROCESSOR DECOUPLING

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Timing Diagram for S5 to S0 mode



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	07	HW	11/19	Compal	PM_DRAM_PWRGD connection is wrong	RC18.2 PM_DRAM_PWRGD change PM_DRAM_PWRGD_A	X01(0.2)
2	15	HW	11/19	Compal	Follow CRB	De-populate CD58	X01(0.2)
3	45	HW	11/19	Compal	For mSATA spec define, remove 1.5V_RUN	Remove C609, C620	X01(0.2)
4	48	HW	11/19	Compal	For ESD request	De-populate C695, C696	X01(0.2)
5	51	HW	11/19	Compal	Due to BIOS code ready	De-populate R1986,R1197,R1118	X01(0.2)
6	30	ME	12/25	Compal	Due to ME request	Swap JLVDS1 pin	X01(0.2)
7	43	HW	12/25	Compal	Follow Intel DG 1.5	Change pin4,7,11	X01(0.2)
8	11	HW	12/25	Compal	Follow Intel DG 1.5	De-populate CC33, CC34, CC36, CC37, CC38, CC39, CC40, CC42, CC43, CC161, CC163, CC165, CC162, CC168, CC169, CC170, CC171,CC167	X01(0.2)
9	23	HW	12/25	Compal	TLS	De-populate RH231, populate RH229	X01(0.2)
10	19	HW	12/25	Compal	Deep sleep	De-populate RH79,RH91, populate RH101, R802, RH75, R808	X01(0.2)
11	42	HW	12/26	Compal	USB charger solution change	Change from SLGC55584AVTR to SLG55594AVTR	X01(0.2)
12	39	HW	12/26	Compal	Due to EA test change 0ohm to 12nH	L63~L70 change from 0ohm to 0603CS-120EJTS	X01(0.2)
13	39	HW	12/26	Compal	Due to CPU +VCCIO_OUT has 6k noise	Populate CC66, and change to 1uf	X01(0.2)
14	20	HW	12/26	Compal	For crystal test	CH13,CH14 change to 12pF	X01(0.2)
15	39	HW	12/26	Compal	For crystal test	C470 change to 22pF,C471 change to 27pF	X01(0.2)
16	51	HW	12/26	Compal	For crystal test	C741 change to 33pF,C743 change to 27pF	X01(0.2)
17	45	HW	12/27	Compal	Debug card port change	Jmini3 pin8,10,12,14,16,17,19 change to Jmini4	X01(0.2)
18	42	HW	01/05	Compal	Follow Compal common rule	C323,C324 change from 150U_D2_6.3VY_R15M to 220U_6.3V_M	X01(0.2)
19	44	HW	01/05	Compal	Follow Compal common rule	C615 change from 150U_D2_6.3VY_R15M to 220U_6.3V_M	X01(0.2)
20	34	HW	01/05	Compal	Part count reduce (DDC)	Remove U21, C365	X01(0.2)
21	30	HW	01/05	Compal	For DFX request	JLVDS1 Pin8 change to NC	X01(0.2)
22	32	HW	01/05	Compal	For DFX request	JEDP1 Pin8 change to NC	X01(0.2)
23	6	HW	01/05	Compal	FDI function test pass, remove reserve component	Remove RC3,RC87, connect directly	X01(0.2)
24	7	HW	01/05	Compal	Part reduce, change reserve resistors to test points	Remove RC30,RC31,RC33,RC34,RC36,RC37,RC38,RC39, add test point	X01(0.2)
25	17	HW	01/07	Compal	MXM function test pass, remove reserve component	Remove R1976, connect directly R1970 change to short pad	X01(0.2)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
26	17	HW	01/07	Compal	P5 did not support GC6	Remove R198,R199, add test point	X01(0.2)
27	34,36	HW	01/07	Compal	DDC function test pass, remove reserve component	Remove R1538,R1523,R2162,R2163	X01(0.2)
28	23	HW	01/07	Compal	PCH function test pass, remove reserve component	RH219 change to short pad	X01(0.2)
29	37	HW	01/07	Compal	HDD function test pass, remove reserve component	Remove R1635,R1636, connect directly	X01(0.2)
30	39	HW	01/07	Compal	LAN function test pass, remove reserve component	Remove R1187,R551,R552, connect directly	X01(0.2)
31	51	HW	01/07	Compal	KBC function test pass, remove reserve component	Remove R853,R840, connect directly	X01(0.2)
32	50	HW	01/07	Compal	SIO function test pass, remove reserve component	Remove R866, connect directly	X01(0.2)
33	44	HW	01/07	Compal	WLAN function test pass, remove reserve component	Remove R702,R707,R703, connect directly	X01(0.2)
34	45	HW	01/07	Compal	Pink Pather function test pass, remove reserve component	Remove R730,R713, connect directly	X01(0.2)
35	44	HW	01/07	Compal	WWAN function test pass, remove reserve component	Remove R703, connect directly	X01(0.2)
36	43	HW	01/07	Compal	Don't support O2 smart card, remove pop option	Remove R220	X01(0.2)
37	54	HW	01/07	Compal	Change for inrush current	C774 change from 2200pf to 0.01uf Add R944 use 20kohm	X01(0.2)
38	30,41,42	EMI	01/07	Compal	For EMI request	L10, L39, L51, L41 change from DLW21SN121SQ2L to DLW21HN900SQ2L	X01(0.2)
39	33	EMI	01/07	Compal	For EMI request	L1, L2, L3 change from BLM18BB470SN1D to BLM15BB470SN1D L4, L5 change from BLM18AG121SN1D to BLM15AG121SN1D	X01(0.2)
40	43	HW	01/07	Compal	Don't support O2 smart card, remove pop option	Remove R221, connect directly	X01(0.2)
41	28	HW	01/07	DELL	Remove 130W protection SW circuitry	Remove U60, R2180~R2187	X01(0.2)
42	44	HW	01/07	Compal	Follow connector list	JSIM1 change from T-SOL 159-1000302600 to T-SOL 159-1000302602	X01(0.2)
43	23,43	HW	01/07	Compal	Follow GPIO3.0C	Add R2195 reserved for SP_TPM_LPC_EN move from ECEOUT65 Net name set to PCH_TPM_EN	X01(0.2)
44	30,50	ESD	01/07	Compal	ESD request	Remove D86,D87,C749,C750	X01(0.2)
45	40	HW	01/07	Compal	LAN function test pass, remove reserve component	Remove C500,C501,C502,C503	X01(0.2)
46	13,14,15,16	HW	01/07	Compal	DDR function test pass, remove reserve component	Remove RD12,RD9,RD17,RD18,RD28,RD29,RD35,RD38	X01(0.2)
47	17	HW	01/07	Compal	Part count reduce (MXM)	De-populate C90,C92,C94,C95,C96	X01(0.2)
48	30	HW	01/07	Compal	Part count reduce (LVDS)	De-populate C726	X01(0.2)
49	36	HW	01/07	Compal	Part count reduce (HDMI)	De-populate C437	X01(0.2)
50	43	HW	01/07	Compal	Part count reduce (TPM)	De-populate C551	X01(0.2)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
51	17	HW	01/07	Compal	Part count reduce (LAN)	De-populate C478	X01 (0.2)
52	53	HW	01/07	Compal	Drop BT feature	De-populate R1133,R1134,C748,C753,R904,C756,C758,R694	X01 (0.2)
53	30	HW	01/07	Compal	Part count reduce (CAMERA)	De-populate C300	X01 (0.2)
54	45	HW	01/07	Compal	Drop Pink Pather function	De-populate C626,C636,C634,C624,C637,C638,C633	X01 (0.2)
55	46	HW	01/07	Compal	For GPIO Map 3.0C	Add populate RH218, de-populate RH214	X01 (0.2)
56	41	HW	01/07	Compal	Add for ESATA repeater 2nd source	Add populate R840,R851, add de-populate R852,R853	X01 (0.2)
57	37	HW	01/07	Compal	Add for HDD repeater 2nd source	Add de-populate R83,R84,R85,R90	X01 (0.2)
58	30	ESD	01/08	Compal	ESD request	Remove D13	X01 (0.2)
59	33	ESD	01/08	Compal	ESD request	Remove D10,D11	X01 (0.2)
60	30	HW	01/08	Compal	For LCDVDD power SW 2nd source	Remove C728 and U28 pin4 connect to +3.3V_ALW	X01 (0.2)
61	35	HW	01/09	Compal	Remove reserve circuit of RTD2136S	Remove U24,R1987,R1988,R1997,R1998	X01 (0.2)
62	51	HW	01/12	Compal	BOARD ID change	R875 change to 130k	X01 (0.2)

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1	57	PWR	11/29/2012	COMPAL	For 1.35V selector	Unpop PR225, PR224, PR218, PR220, PR217, PR211, PR222, PR223, PC217 PQ205, PR221, PC220, PR216, PR219, PC219, PQ204, PR213, PC216	X01
2	56	PWR	11/29/2012	COMPAL	For 3.3V OCP setting	Change PR105 to 90.9K	X01
3	57	PWR	11/29/2012	COMPAL	For 1.5V output voltage setting	Change PR402 to 30.1K, PR405 to 20K	X01
4	56	PWR	11/29/2012	COMPAL	For 3.3V/5V output voltage setting	Change PR102 and PR104 to 10K 1%	X01
5	58	PWR	11/29/2012	COMPAL	Change better Vcore MOSFET	Change PQ500, PQ501, PQ502, PQ503, PQ504, PQ505 to CSD87350Q5D	X01
6	55	PWR	12/11/2012	COMPAL	Main source have x1 code	Change PQ1, PQ1070 to SB00000H500	X01
7	55	PWR	12/11/2012	COMPAL	Main source have x1 code	Change PU1 to SA00003DN00	X01
8	61	PWR	12/11/2012	COMPAL	For part count reduction	Combine PQ708, PQ709 to SB00000DH0L	X01
9	58	PWR	12/11/2012	COMPAL	For part count reduction	Unpop PC304, change PC305 to SE00000QK00	X01
10	57	PWR	12/11/2012	COMPAL	For part count reduction	Unpop PC208, change PC207 to SE000008L80	X01
11	55	PWR	12/20/2012	COMPAL	Unite to same part number	Change PQ1, PQ1070 to SB000007900	X01
12	57	PWR	12/21/2012	COMPAL	For cost down	Change PL201 to SH000004S00, PL701 to SH00000PO00	X01
13	62	PWR	12/26/2012	COMPAL	For Japan's Energy star	Add PQ1072, PQ1011, PD1010, PR1030, PD1100, PR1100, PR1031, PR1032	X01
14	62	PWR	12/26/2012	COMPAL	For boost charger behavior	Add PR1026, PQ1083	X01
15	61	PWR	12/26/2012	COMPAL	For current sense accuracy	Change PR706=33.2ohm, PR708=6.8ohm, PR713=12.1ohm, PR715=20ohm	X01
16	60	PWR	01/03/2013	COMPAL	For Vcore compensation	Add PR558=5.1Mohm, PR537=619ohm, PR521=93.1Kohm, PC509=820pF	X01
17	60	PWR	01/03/2013	COMPAL	For EMI request	Pop PC516=470pF	X01
18	61	PWR	01/07/2013	COMPAL	Unite to same part number	Change PD703 to SCS0340L010	X01
19	55	PWR	01/07/2013	COMPAL	Change to small size bead	Change PL3 to SM01000MB00	X01
20	61	PWR	01/08/2013	COMPAL	Refer to E5	Change PR737.1 to +3.3V_ALW2	X01
21	56	PWR	01/10/2013	COMPAL	To improve 3.3V low side induce voltage	Reserve PC199= 56pF_0402_50V	X01

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PWR P.I.R (1/1)

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